

36Mb NTSRAM Flow-Through Specification

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Document Title

1Mx36 & 2Mx18 Bit NTSRAM Flow-Through

Revision History

Rev. No.	History	Draft Date	Remark
1.0	Final spec release	May 2013	Final
1.1	Change tHZOE value from 3.5 to 3.2	Oct. 2014	Final

S7M323635M S7M321835M

1Mx36 & 2Mx18 NTSRAM Flow-Through

1Mx36 & 2Mx18 Bit NTSRAM Flow-Through

Features

- Fully registered inputs and outputs for pipelined operation
- $V_{DD} = 2.5V(2.3V \sim 2.7V)$ or $3.3V(3.1V \sim 3.5V)$ Power Supply
- $V_{DDQ} = 2.3V \sim 2.7V$ I/O Power Supply ($V_{DD} = 2.5V$) or $2.3V \sim 3.5V$ I/O Power Supply ($V_{DD} = 3.3V$)
- Byte Writable Function
- Enable clock and suspend operation
- Single Read/Write control pin
- Asynchronous output enable control
- Self-timed Write control
- Three Chip Enable for simple depth expansion with no data contention
- An interleaved burst or a linear burst mode
- Power Down mode
- Operating in commercial and industrial temperature range
- 100-TQFP-1420A (Lead free package)

General Description

The S7M323635M and S7M321835M are 37,748,736-bit Synchronous Static SRAMs. The NTSRAM, or Non-Turnaround Static Random Access Memory utilizes all bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock.

Burst order control must be tied "High or Low". Asynchronous inputs include the sleep mode enable(ZZ). Output Enable controls the outputs at any given time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals. For read cycles, Flow-Through SRAM allows output data to simply flow freely from the memory array.

The S7M323635M and S7M321835M are implemented with high performance CMOS technology and is available in 100pin TQFP and Multiple power and ground pins minimize ground bounce.

Key Parameters

Parameter	Symbol	-65	-75	Unit
Cycle Time	tCYC	7.5	8.5	ns
Clock Access Time	tCD	6.5	7.5	ns
Output Enable Access Time	tOE	3.2	3.2	ns
Operating Current	I _{cc}	220	210	mA
Standby Current	I _{SB2}	120	120	mA

36Mb NTSRAM Flow-Through Ordering Information

Org.	VDD (V)	Speed (ns)	Access Time (ns)	Part Number	RoHS Avail.
2Mx18	3.3/2.5	7.5	6.5	S7M321835M-PC(I)65	0
	3.3/2.5	8.5	7.5	S7M321835M-PC(I)75	0
1Mx36	3.3/2.5	7.5	6.5	S7M323635M-PC(I)65	0
	3.3/2.5	8.5	7.5	S7M323635M-PC(I)75	0

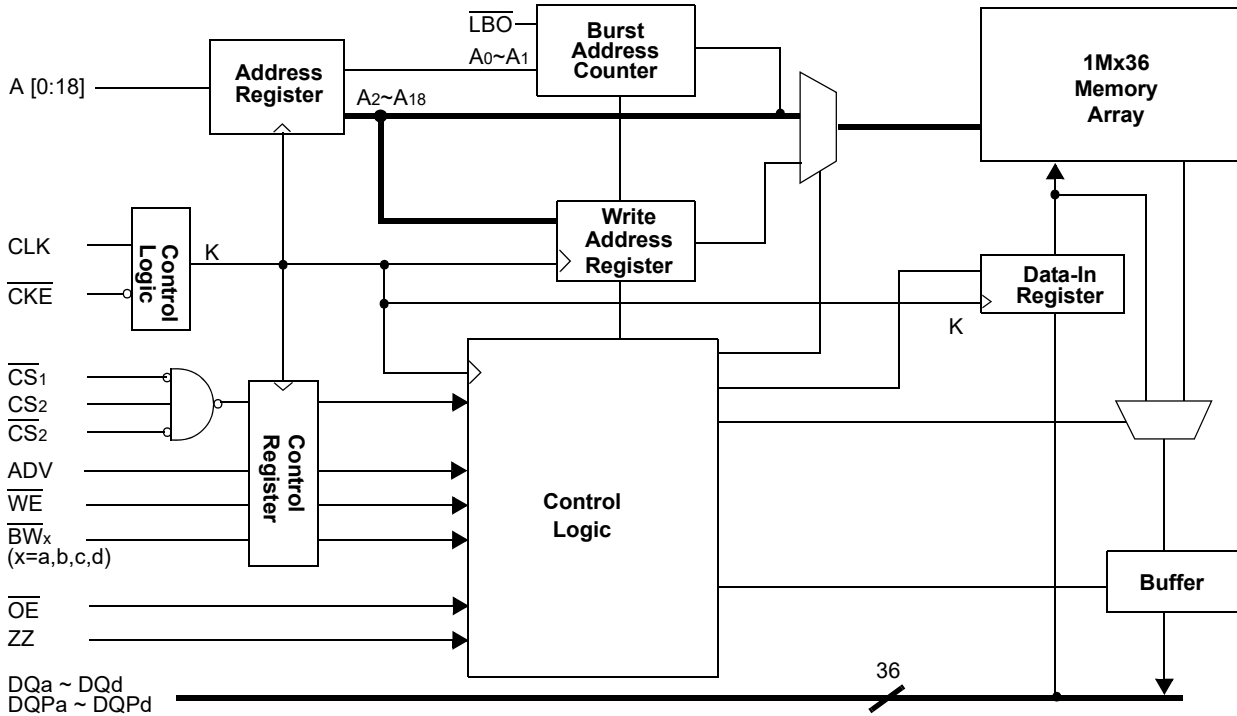
Note 1. P [Package type] : P - Pb Free

2. C(I) [Operating Temperature] : C-Commercial, I-Industrial

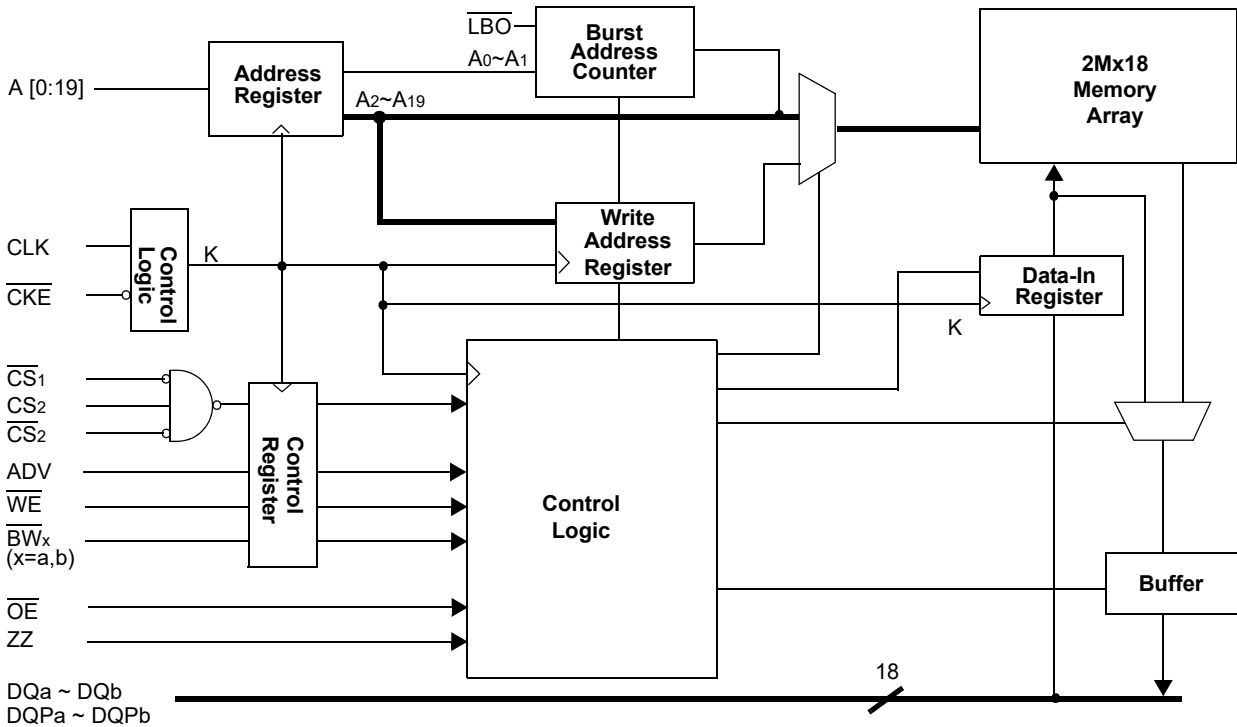
S7M323635M
S7M321835M

1Mx36 & 2Mx18 NTSRAM Flow-Through

Logic Block Diagram - S7M323635M (1M x 36)



Logic Block Diagram - S7M321835M (2M x 18)



Function Description

The S7M323635M and S7M321835M are NTSRAM designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.

All inputs (with the exception of \overline{OE} , \overline{LBO} and \overline{ZZ}) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable(\overline{CKE}) pin allows the operation of the chip to be suspended as long as necessary. When \overline{CKE} is high, all synchronous inputs are ignored and the internal device registers will hold their previous values.

NTSRAM latches external address and initiates a cycle, when \overline{CKE} , ADV are driven to low and all three chip enables($\overline{CS1}$, $CS2$, $\overline{CS2}$) are active . Output Enable(\overline{OE}) can be used to disable the output at any given time.

Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, CKE is driven low, all three chip enables($\overline{CS1}$, $CS2$, $\overline{CS2}$) are active, the write enable input signals WE are driven high, and ADV driven low. Data appears at the outputs within the same clock cycle as the address for the data. Also during read operation OE must be driven low for the device to drive out the requested data.

Write operation occurs when WE is driven low at the rising edge of the clock. BW[d:a] can be used for byte write operation. The Flow Through NTSRAM uses a late write cycle to utilize 100% of the bandwidth.

At the first rising edge of the clock, WE and address are registered, and the data associated with that address is required one cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

The burst sequence is determined by the state of the LBO pin. When this pin is low, linear burst sequence is selected.

And when this pin is high, Interleaved burst sequence is selected.

During normal operation, \overline{ZZ} must be driven low. When \overline{ZZ} is driven high, the SRAM will enter a Power Sleep Mode after 2 cycles.

At this time, internal state of the SRAM is preserved. When \overline{ZZ} returns to low, the SRAM normally operates after 2 cycles of wake up time.

Burst Sequence Table

(Interleaved Burst, \overline{LBO} =High)

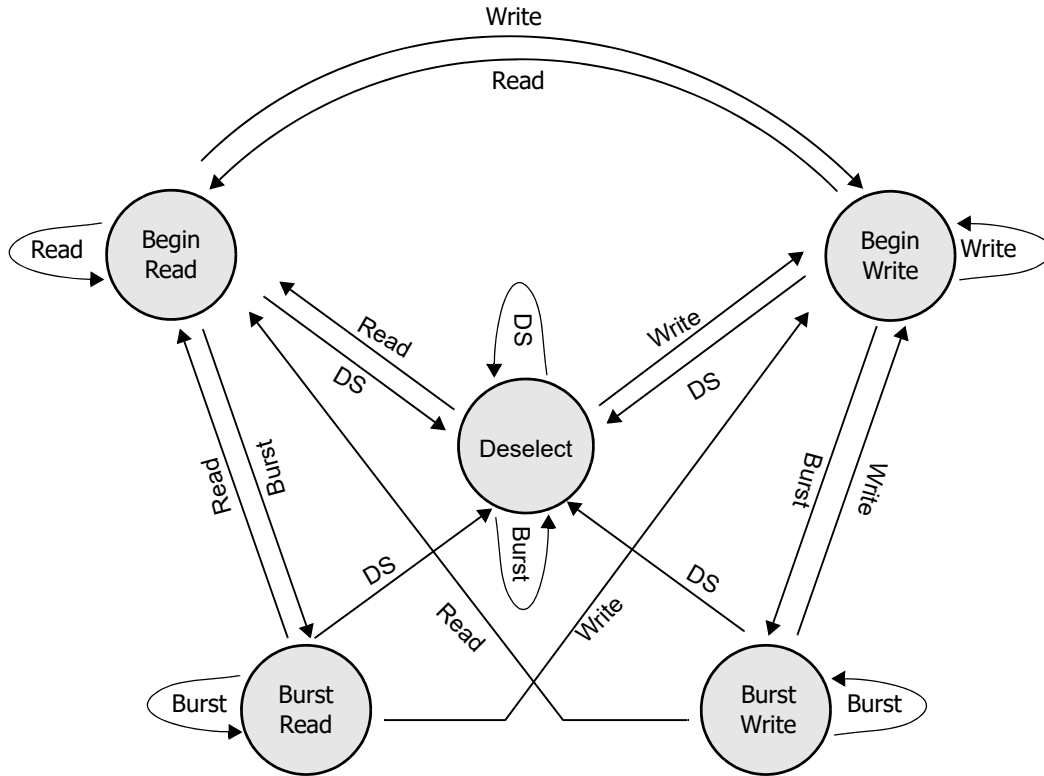
\overline{LBO} PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst, \overline{LBO} =Low)

\overline{LBO} PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

Note : 1. \overline{LBO} pin must be tied to High or Low, and Floating State must not be allowed.

State Diagram For NTSRAM



Command	Action
DS	Deselect
Read	Begin Read
Write	Begin Write
Burst	Begin Read Begin Write Continue Deselect

Notes : 1. An Ignore Clock Edge cycle is not shown in the above diagram. This is because CKE HIGH only blocks the clock(CLK) input and does not change the state of the device.
2. States change on the rising edge of the clock(CLK)

Truth Tables

Synchronous Truth Table

\overline{CS}_1	CS_2	\overline{CS}_2	ADV	\overline{We}	\overline{BW}_x	\overline{OE}	\overline{CKE}	CLK	Address Accessed	Operation
H	X	X	L	X	X	X	L	↑	N/A	Not Selected
X	L	X	L	X	X	X	L	↑	N/A	Not Selected
X	X	H	L	X	X	X	L	↑	N/A	Not Selected
X	X	X	H	X	X	X	L	↑	N/A	Not Selected Continue
L	H	L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	X	X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	H	L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	X	X	H	X	X	H	L	↑	Next Address	Dummy Read
L	H	L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	X	X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	H	L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	X	X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	X	X	H	↑	Current Address	Ignore Clock

- Notes :**
1. X means "Don't Care".
 2. The rising edge of clock is symbolized by (↑).
 3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
 4. $\overline{We} = L$ means Write operation in Write Truth Table.
 $\overline{We} = H$ means Read operation in Write Truth Table.
 5. Operation finally depends on status of asynchronous input pins(ZZ and \overline{OE}).

Write Truth Table(x36)

\overline{WE}	\overline{BW}_a	\overline{BW}_b	\overline{BW}_c	\overline{BW}_d	Operation
H	X	X	X	X	Read
L	L	H	H	H	Write Byte a
L	H	L	H	H	Write Byte b
L	H	H	L	H	Write Byte c
L	H	H	H	L	Write Byte d
L	L	L	L	L	Write All Bytes
L	H	H	H	H	Write Abort/NOP

- Notes :**
1. X means "Don't Care".
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

Write Truth Table(x18)

\overline{WE}	\overline{BW}_a	\overline{BW}_b	Operation
H	X	X	Read
L	L	H	Write Byte a
L	H	L	Write Byte b
L	L	L	Write All Bytes
L	H	H	Write Abort/NOP

- Notes :**
1. X means "Don't Care".
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

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Asynchronous Truth Table

Operation	ZZ	\overline{OE}	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. Sleep Mode means power Sleep Mode of which stand-by current does not depend on cycle time.
3. Deselected means power Sleep Mode of which stand-by current depends on cycle time.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on V _{DD} Supply Relative to V _{SS}	V _{DD}	-0.5 to 4.6	V
Voltage on Any Other Pin Relative to V _{SS}	V _{IN}	-0.5 to V _{DD} +0.3	V
Power Dissipation	P _D	1.4	W
Storage Temperature	T _{STG}	-65 to 150	°C
Operating Temperature	Commercial	T _{OPR}	0 to 70
	Industrial	T _{OPR}	-40 to 85
Storage Temperature Range Under Bias	T _{BIAS}	-10 to 85	°C

Latch up current >200mA

Notes : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions (0°C ≤ T_A ≤ 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V _{DD1}	2.3	2.5	2.7	V
	V _{DDQ1}	2.3	2.5	2.7	V
	V _{DD2}	3.1	3.3	3.5	V
	V _{DDQ2}	2.3	3.3	3.5	V
Ground	V _{SS}	0	0	0	V

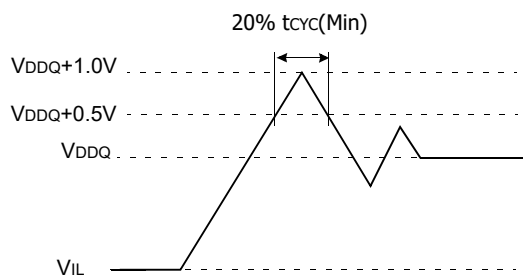
- Notes:** 1. The above parameters are also guaranteed at industrial temperature range.
2. It should be V_{DDQ} ≤ V_{DD}

Capacitance (T_A=25°C, f=1MHz)

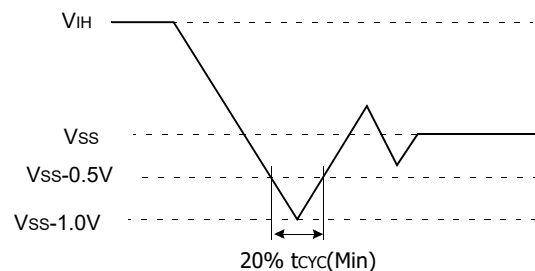
Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C _{IN}	V _{IN} =0V	-	5	pF
Output Capacitance	C _{OUT}	V _{OUT} =0V	-	7	pF

Note : Sampled not 100% tested.

Overshoot Timing



Undershoot Timing



DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit	Notes	
Input Leakage Current(except ZZ)	IIL	VDD=Max ; VIN=VSS to VDD	-2	+2	uA		
Output Leakage Current	IOL	Output Disabled, Vout=VSS to VDDQ	-2	+2	uA		
Operating Current	ICC	Device Selected, IOUT=0mA, ZZ ≤ VIL , Cycle Time ≥ tcyc Min	-65	-	220	mA	1,2
			-75	-	210		
Standby Current	ISB	Device deselected, IOUT=0mA, ZZ ≤ VIL, f=Max, All Inputs ≤ VIL or ≥ VIH	-	125	mA		
	ISB1	Device deselected, IOUT=0mA, ZZ ≤ 0.2V, f=0, All Inputs=fixed (VDD-0.2V or 0.2V)	-	120	mA		
	ISB2	Device deselected, IOUT=0mA, ZZ ≥ VDD-0.2V, f=Max, All Inputs ≤ VIL or ≥ VIH	-	120	mA		
Output Low Voltage(3.3V I/O)	VoL	IOL=8.0mA	-	0.4	V		
Output High Voltage(3.3V I/O)	VoH	IOH=-4.0mA	2.4	-	V		
Output Low Voltage(2.5V I/O)	VoL	IOL=1.0mA	-	0.4	V		
Output High Voltage(2.5V I/O)	VoH	IOH=-1.0mA	2.0	-	V		
Input Low Voltage(3.3V I/O)	VIL		-0.3*	0.8	V		
Input High Voltage(3.3V I/O)	VIH		2.0	VDD+0.3**	V	3	
Input Low Voltage(2.5V I/O)	VIL		-0.3*	0.7	V		
Input High Voltage(2.5V I/O)	VIH		1.7	VDD+0.3**	V	3	

Notes : The above parameters are also guaranteed at industrial temperature range.
 1. Reference AC Operating Conditions and Characteristics for input and timing.
 2. Data states are all zero.
 3. In Case of I/O Pins, the Max. VIH=VDDQ+0.3V

Test Conditions

Parameter	Value
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3/2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	VDDQ/2
Output Load	See Fig. 1

The above parameters are also guaranteed at industrial temperature range.

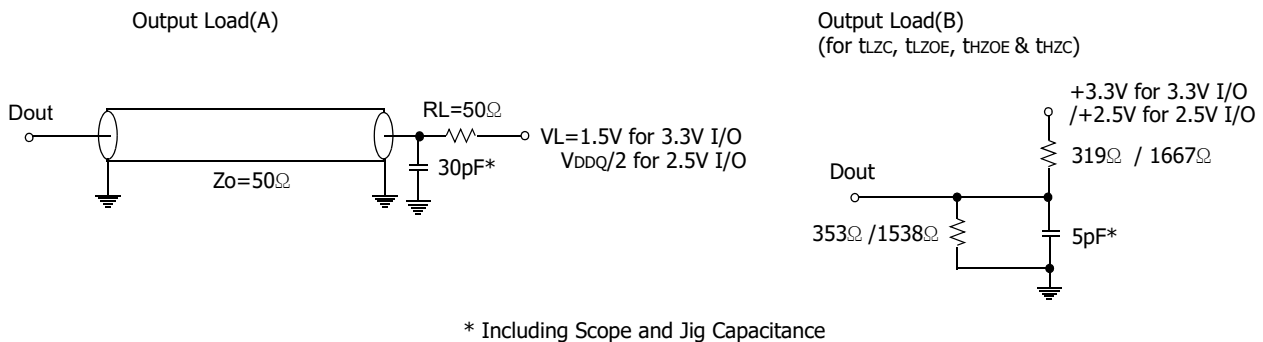


Fig. 1

AC Timing Characteristics

Parameter	Symbol	-65		-75		Unit
		Min	Max	Min	Max	
Cycle Time	t _{CYC}	7.5	-	8.5	-	ns
Clock Access Time	t _{CD}	-	6.5	-	7.5	ns
Output Enable to Data Valid	t _{OE}	-	3.2	-	3.2	ns
Clock High to Output Low-Z	t _{LZC}	2.5	-	2.5	-	ns
Output Hold from Clock High	t _{OH}	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	t _{LZOE}	0	-	0	-	ns
Output Enable High to Output High-Z	t _{HZOE}	-	3.2	-	3.2	ns
Clock High to Output High-Z	t _{HZC}	-	3.8	-	4.0	ns
Clock High Pulse Width	t _{CH}	2.5	-	2.8	-	ns
Clock Low Pulse Width	t _{CL}	2.5	-	2.8	-	ns
Address Setup to Clock High	t _{AS}	1.5	-	1.5	-	ns
$\overline{\text{CKE}}$ Setup to Clock High	t _{CES}	1.5	-	1.5	-	ns
Data Setup to Clock High	t _{DS}	1.5	-	1.5	-	ns
Write Setup to Clock High ($\overline{\text{WE}}$, $\overline{\text{BWx}}$)	t _{WS}	1.5	-	1.5	-	ns
Address Advance Setup to Clock High	t _{ADVS}	1.5	-	1.5	-	ns
Chip Select Setup to Clock High	t _{CSS}	1.5	-	1.5	-	ns
Address Hold from Clock High	t _{AH}	0.5	-	0.5	-	ns
$\overline{\text{CKE}}$ Hold from Clock High	t _{CEH}	0.5	-	0.5	-	ns
Data Hold from Clock High	t _{DH}	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{\text{WE}}$, $\overline{\text{BWx}}$)	t _{WH}	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t _{ADVH}	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t _{CSH}	0.5	-	0.5	-	ns
ZZ High to Power Down	t _{PDS}	2	-	2	-	cycle
ZZ Low to Power Up	t _{PUS}	2	-	2	-	cycle

- Notes :**
1. The above parameters are also guaranteed at industrial temperature range.
 2. All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and $\overline{\text{CS}}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
 3. Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
 4. A write cycle is defined by $\overline{\text{WE}}$ low having been registered into the device at ADV Low, A Read cycle is defined by $\overline{\text{WE}}$ High with ADV Low, Both cases must meet setup and hold times.
 5. To avoid bus contention, At a given voltage and temperature t_{LZC} is more than t_{HZC}.
 The specs as shown do not imply bus contention because t_{LZC} is a Min. parameter that is worst case at totally different test conditions (0 °C; 3.5V) than t_{HZC}, which is a Max. parameter(worst case at 70 °C; 3.1V)
 It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

Sleep Mode

Sleep Mode is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2} . The duration of Sleep Mode is dictated by the length of time the ZZ is in a High state.

After entering Sleep Mode, all inputs except ZZ become disabled and all outputs go to High-Z.

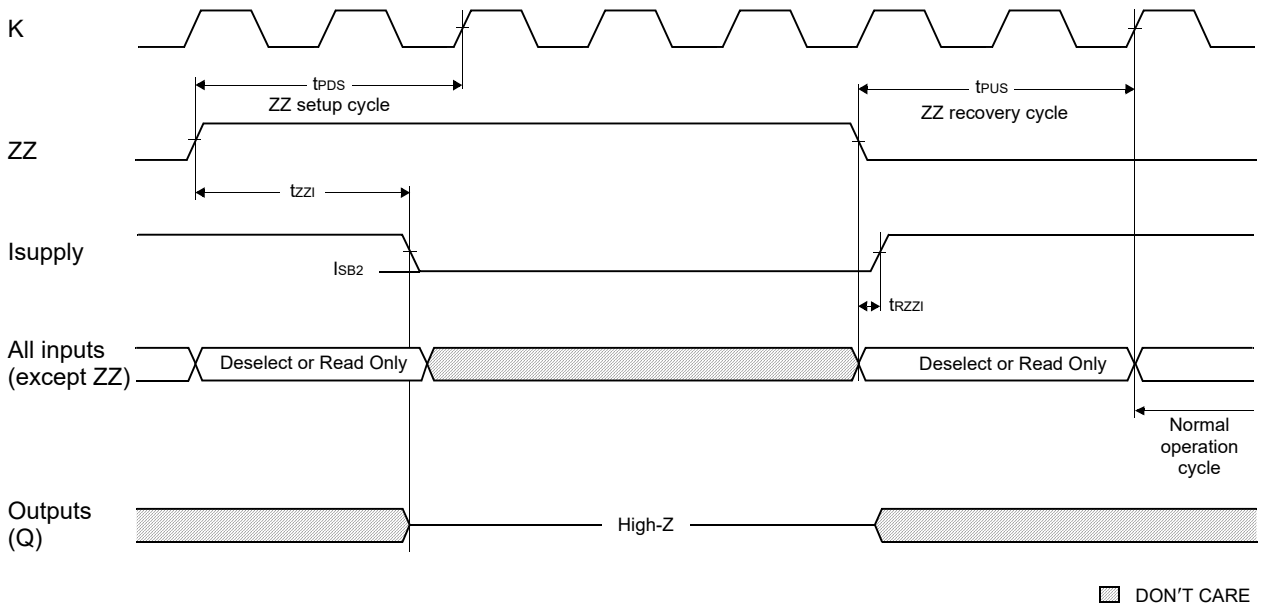
The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep Mode.

When the ZZ pin becomes a logic High, I_{SB2} is guaranteed after the time t_{ZZI} is met. Any operation pending when entering Sleep Mode is not guaranteed to successful complete. Therefore, Sleep Mode (Read or Write) must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep Mode during t_{PUS} , only a Deselect or Read cycle should be given while the SRAM is transitioning out of Sleep Mode.

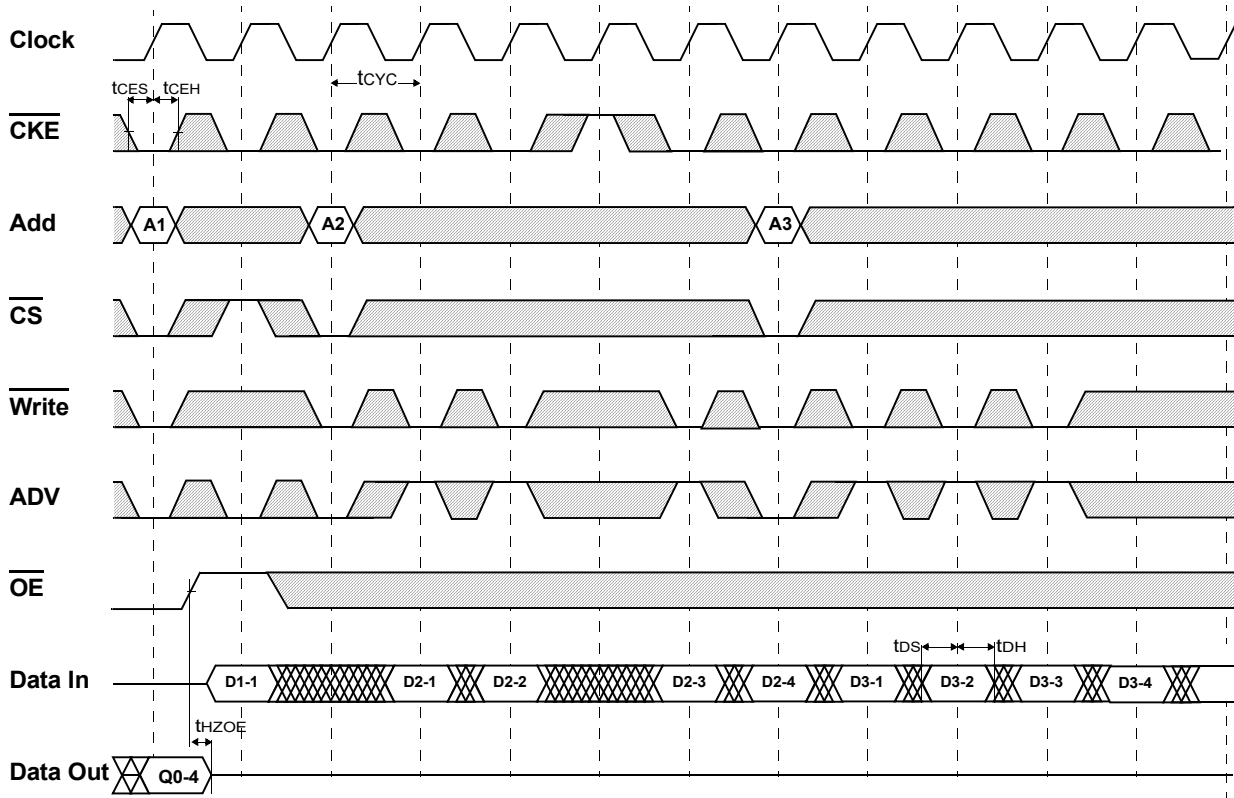
Sleep Mode Electrical Characteristics

Description	Condition	Symbol	Min	Max	Unit
Current during SLEEP MODE	$ZZ \geq V_{IH}$	I_{SB2}		120	mA
ZZ active to input ignored		t_{PDS}	2		cycle
ZZ inactive to input sampled		t_{PUS}	2		cycle
ZZ active to SLEEP current		t_{ZZI}		2	cycle
ZZ inactive to exit SLEEP current		t_{RZZI}	0		

Sleep Mode Waveform



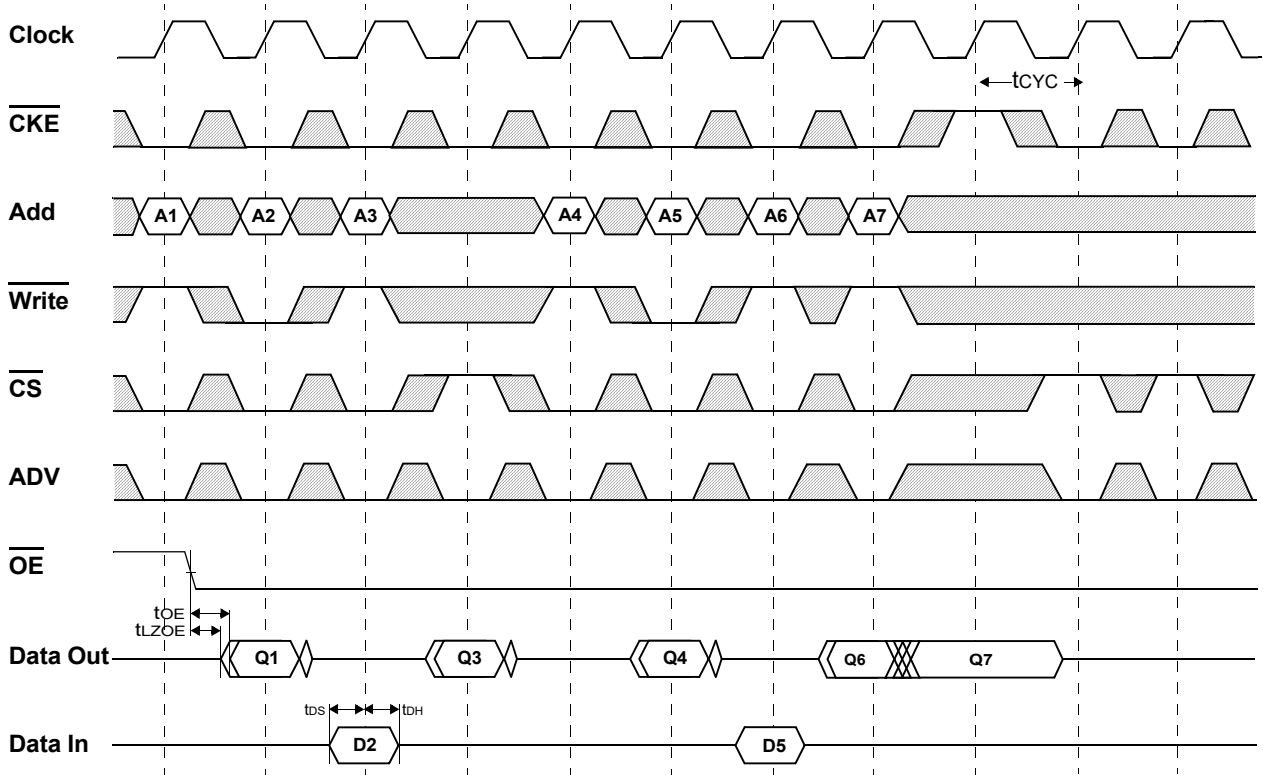
Timing Waveform Of Write Cycle



NOTES : $\overline{\text{Write}} = \text{L}$ means $\overline{\text{WE}} = \text{L}$, and $\overline{\text{BWx}} = \text{L}$
 $\overline{\text{CS}} = \text{L}$ means $\overline{\text{CS}}_1 = \text{L}$, $\text{CS}_2 = \text{H}$ and $\overline{\text{CS}}_2 = \text{L}$
 $\overline{\text{CS}} = \text{H}$ means $\overline{\text{CS}}_1 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$ and $\overline{\text{CS}}_2 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$, and $\text{CS}_2 = \text{L}$

□ Don't Care
 ⊗ Undefined

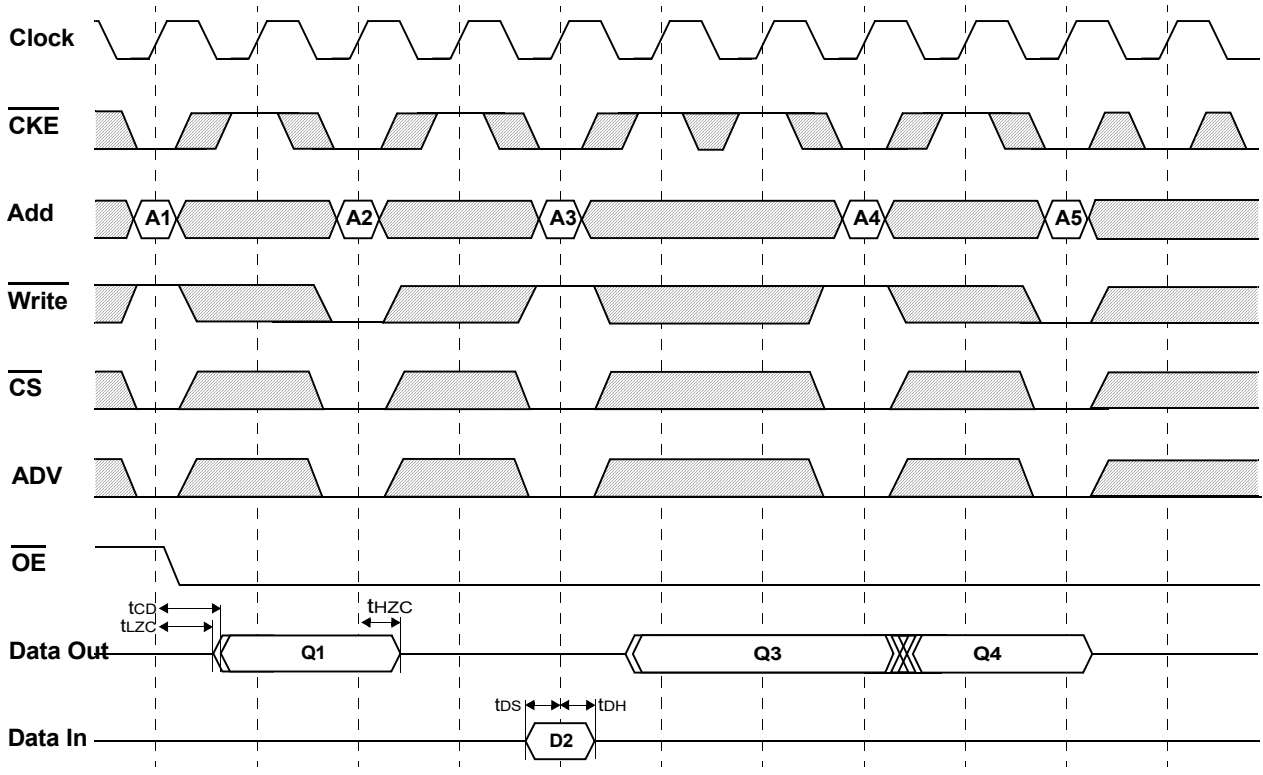
Timing Waveform Of Single Read/Write



NOTES: $\overline{\text{Write}} = L$ means $\overline{\text{WE}} = L$, and $\overline{\text{BWx}} = L$
 $\overline{\text{CS}} = L$ means $\overline{\text{CS}}_1 = L$, $\text{CS}_2 = H$ and $\overline{\text{CS}}_2 = L$
 $\overline{\text{CS}} = H$ means $\overline{\text{CS}}_1 = H$, or $\overline{\text{CS}}_1 = L$ and $\text{CS}_2 = H$, or $\overline{\text{CS}}_1 = L$, and $\text{CS}_2 = L$

□ Don't Care
 ▣ Undefined

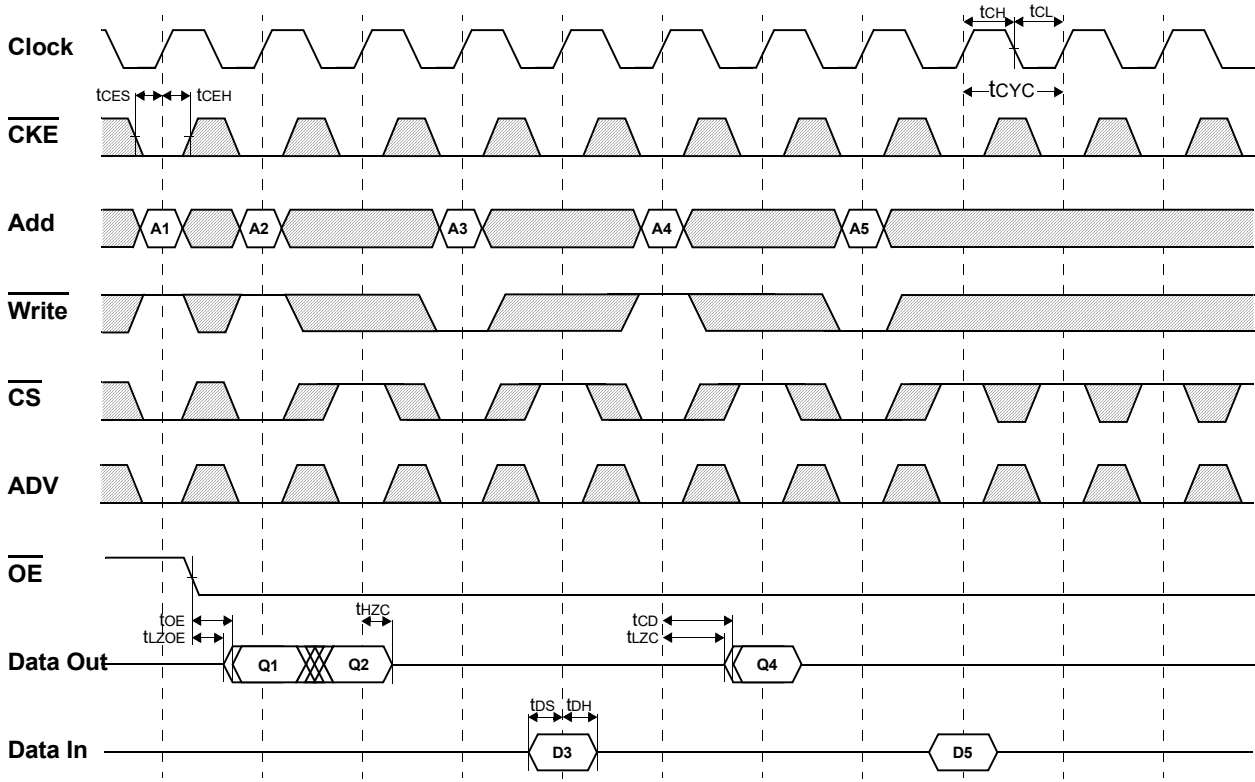
Timing Waveform Of $\overline{\text{CKE}}$ Operation



NOTES : $\overline{\text{Write}} = \text{L}$ means $\overline{\text{WE}} = \text{L}$, and $\overline{\text{BWx}} = \text{L}$
 $\overline{\text{CS}} = \text{L}$ means $\overline{\text{CS}}_1 = \text{L}$, $\text{CS}_2 = \text{H}$ and $\overline{\text{CS}}_2 = \text{L}$
 $\overline{\text{CS}} = \text{H}$ means $\overline{\text{CS}}_1 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$ and $\text{CS}_2 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$, and $\text{CS}_2 = \text{L}$

□ Don't Care
 ⊠ Undefined

Timing Waveform Of \overline{CS} Operation



NOTES : $\overline{Write} = L$ means $\overline{WE} = L$, and $\overline{BWx} = L$
 $\overline{CS} = L$ means $\overline{CS}_1 = L$, $CS_2 = H$ and $\overline{CS}_2 = L$
 $\overline{CS} = H$ means $\overline{CS}_1 = H$, or $\overline{CS}_1 = L$ and $\overline{CS}_2 = H$, or $\overline{CS}_1 = L$, and $CS_2 = L$

□ Don't Care
 ⊠ Undefined

S7M323635M
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1Mx36 & 2Mx18 NTSRAM Flow-Through

Package Dimensions

