

# 4Mb Sync. Flow-Through SRAM Specification

**NETSOL RESERVES THE RIGHT TO CHANGE PRODUCTS, INFORMATION AND SPECIFICATIONS WITHOUT NOTICE.**

Products and specifications discussed herein are for reference purposes only. All information discussed herein is provided on an "AS IS" basis, without warranties of any kind.

This document and all information discussed herein remain the sole and exclusive property of NETSOL. No license of any patent, copyright, mask work, trademark or any other intellectual property right is granted by one party to the other party under this document, by implication, estoppel or otherwise.

For updates or additional information about Netsol products, please contact to [netsol@netsol.co.kr](mailto:netsol@netsol.co.kr)

**Document Title**

128Kx36 & 256Kx18 Bit Flow-Through SRAM

**Revision History**

Rev. No.	History	Draft Date	Remark
0.0	Initial Draft	Aug. 2011	Preliminary
1.0	1. Final Spec Release 2. Insert ICC Parameters	Nov. 2011	Final

**128Kx36 & 256Kx18 Bit Flow-Through SRAM**

**Features**

- V<sub>DD</sub> = 2.5V(2.3V ~ 2.7V) or 3.3V(3.1V ~ 3.5V) Power Supply
- V<sub>DDQ</sub> = 2.3V~2.7V I/O Power Supply (V<sub>DD</sub>=2.5V) or 2.3V~3.5V I/O Power Supply (V<sub>DD</sub>=3.3V)
- Synchronous Operation
- Self-Timed Write Cycle
- On-Chip Address Counter and Control Registers
- Byte Writable Function
- Global Write Enable Controls a full bus-width write
- Power Down State via ZZ Signal
- LBO Pin allows a choice of either a interleaved burst or a linear burst
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP
- Asynchronous Output Enable Control
- ADSP, ADSC, ADV Burst Control Pins
- TTL-Level Three-State Output
- Operating in commercial and industrial temperature range
- 100-TQFP-1420A (Lead free package)

**General Description**

The S7B403635M and S7B401835M are 4,718,592-bit Synchronous Static Random Access Memory designed for high performance.

It is organized as 128K(256K) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance applications;  $\overline{GW}$ ,  $\overline{BW}$ ,  $\overline{LBO}$ ,  $\overline{ZZ}$ . Write cycles are internally self-timed and synchronous.

Full bus-width write is done by  $\overline{GW}$ , and each byte write is performed by the combination of  $\overline{WEx}$  and  $\overline{BW}$  when  $\overline{GW}$  is high. And with  $\overline{CS_1}$  high,  $\overline{ADSP}$  is blocked to control signals.

Burst cycle can be initiated with either the address status processor( $\overline{ADSP}$ ) or address status cache controller( $\overline{ADSC}$ ) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance( $\overline{ADV}$ ) input.

$\overline{LBO}$  pin is DC operated and determines burst sequence(linear or interleaved).

$\overline{ZZ}$  pin controls Power Down State and reduces Stand-by current regardless of CLK.

The S7B403635M and S7B401835M are fabricated using high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

**Key Parameters**

Parameter	Symbol	-65	-75	Unit
Cycle Time	tCYC	7.5	8.5	ns
Clock Access Time	tCD	6.5	7.5	ns
Output Enable Access Time	tOE	3.5	3.5	ns
Operating Current	I <sub>CC</sub>	110	100	mA
Standby Current	I <sub>SB2</sub>	30	30	mA

**4Mb Synchronous Burst SRAM Ordering Information**

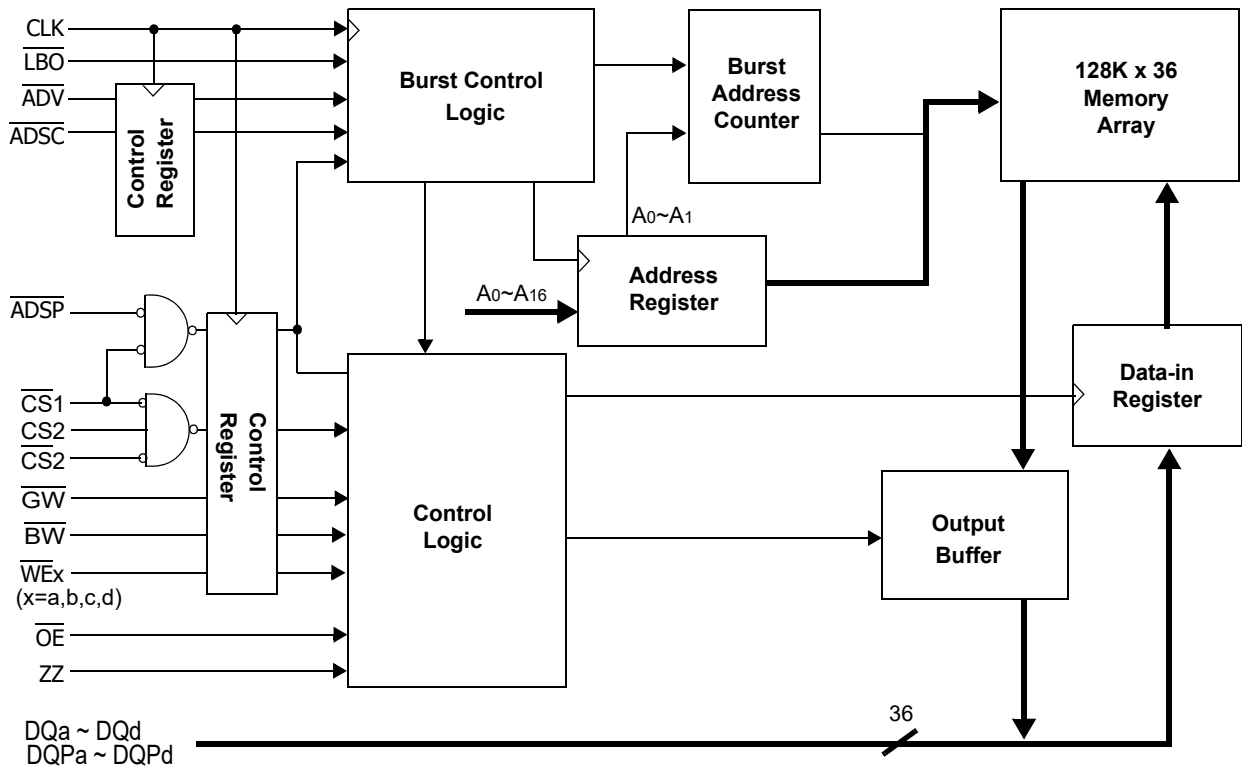
Org.	V <sub>DD</sub> (V)	Speed (ns)	Access Time (ns)	Part Number	RoHS Avail.
256Kx18	3.3/2.5	7.5	6.5	S7B401835M-PC(I)65	0
	3.3/2.5	8.5	7.5	S7B401835M-PC(I)75	0
128Kx36	3.3/2.5	7.5	6.5	S7B403635M-PC(I)65	0
	3.3/2.5	8.5	7.5	S7B403635M-PC(I)75	0

- Note 1. P [Package type] : P - Pb Free  
 2. C(I) [Operating Temperature] : C-Commercial, I-Industrial

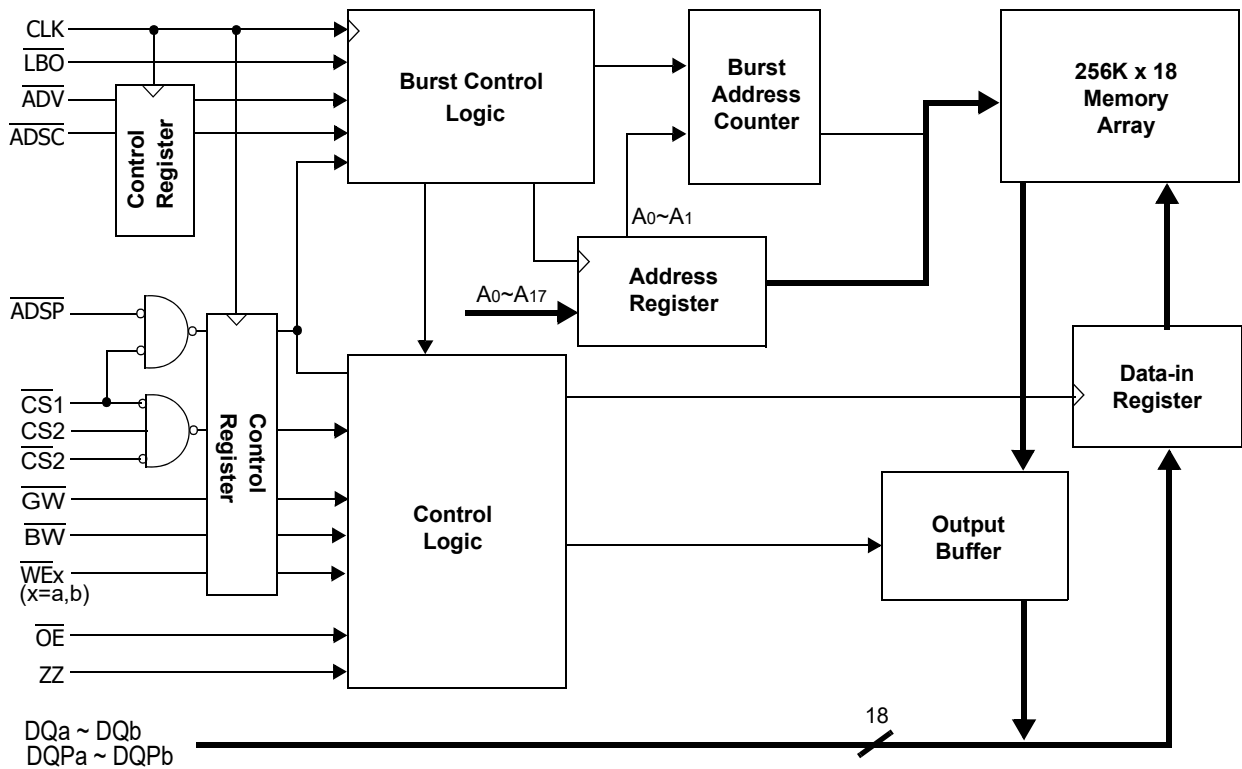
**S7B403635M  
S7B401835M**

**128Kx36 & 256Kx18 Flow-Through SRAM**

**Logic Block Diagram - S7B403635M (128K x 36)**



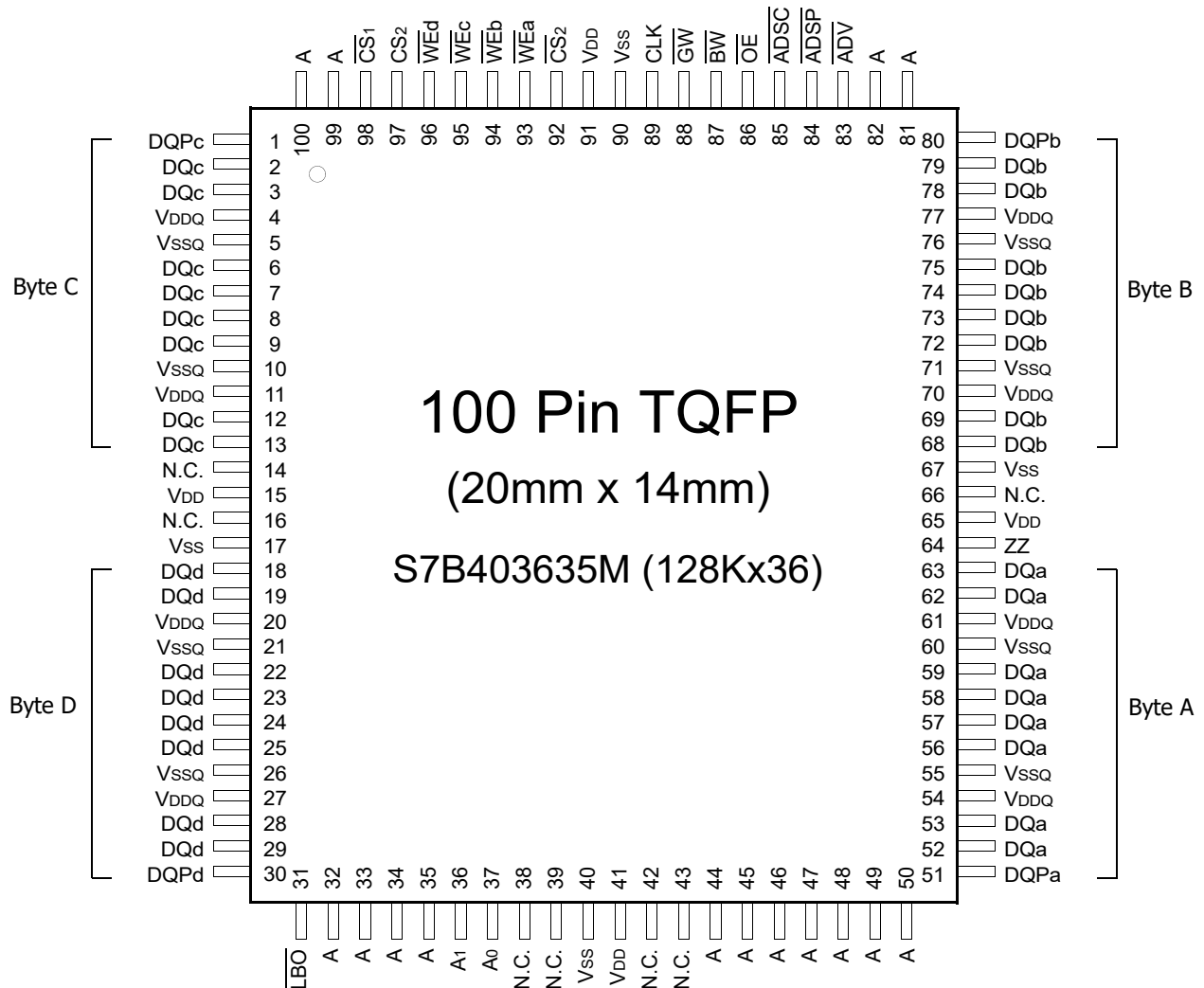
**Logic Block Diagram - S7B401835M (256K x 18)**



**S7B403635M**  
**S7B401835M**

**128Kx36 & 256Kx18 Flow-Through SRAM**

**100 TQFP Package Pin Configurations(Top View)**



**Pin Name**

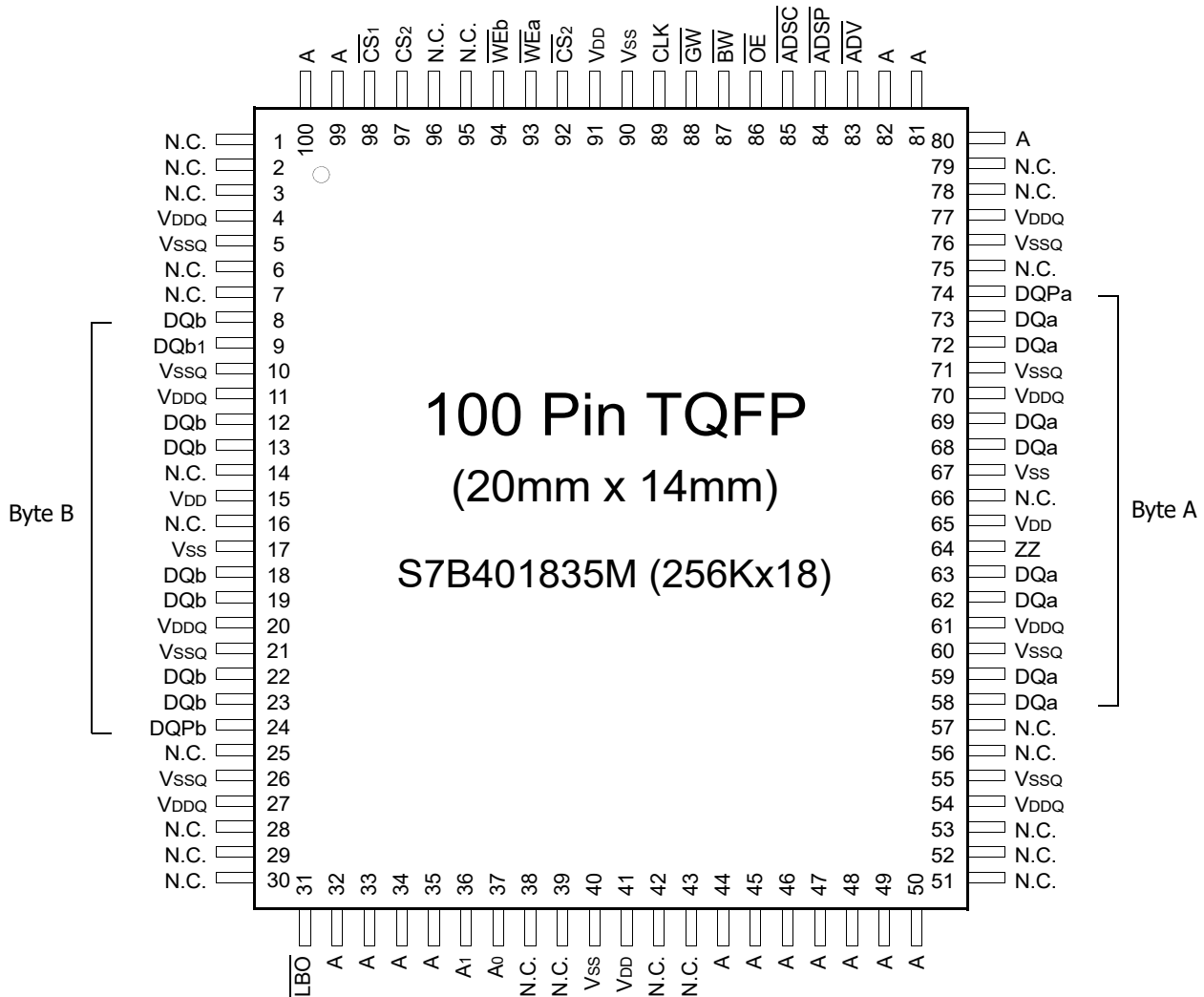
Symbol	Pin Name	TQFP Pin NO.	Symbol	Pin Name	TQFP Pin NO.
A	Address Inputs	32,33,34,35,44,45,46 47,48,49,50,81,82,99 100	VDD	Power Supply (2.5V~3.3V)	15,41,65,91
A0,A1	Burst Address Inputs	37,36	VSS	Ground	17,40,67,90
ADV	Burst Address Advance	83	N.C.	No Connect	14,16,38,39,42,43,66
ADSP	Address Status Processor	84	DQa	Data Inputs/Outputs	52,53,56,57,58,59,62,63 68,69,72,73,74,75,78,79
ADSC	Address Status Controller	85	DQb		2,3,6,7,8,9,12,13
CLK	Clock	89	DQc		18,19,22,23,24,25,28,29
CS1	Chip Select	98	DQd		51,80,1,30
CS2	Chip Select	97	DQP~Pd		
CS2	Chip Select	92	VDDQ	Output Power Supply (2.5V~3.3V)	4,11,20,27,54,61,70,77
WEx(x=a,b,c,d)	Byte Write Inputs	93,94,95,96	VSSQ	Output Ground	5,10,21,26,55,60,71,76
OE	Output Enable	86			
GW	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

Note : 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

**S7B403635M**  
**S7B401835M**

**128Kx36 & 256Kx18 Flow-Through SRAM**

**100 TQFP Package Pin Configurations (Top View)**



**Pin Name**

Symbol	Pin Name	TQFP Pin NO.	Symbol	Pin Name	TQFP Pin NO.
A	Address Inputs	32,33,34,35,44,45,46,47,48,49,50,80,81,82,99,100	VDD	Power Supply (2.5V~3.3V)	15,41,65,91
A0,A1	Burst Address Inputs	37,36	VSS	Ground	17,40,67,90
ADV	Burst Address Advance	83	N.C.	No Connect	1,2,3,6,7,14,16,25,28,29
ADSP	Address Status Processor	84			30,38,39,42,43,51,52,53
ADSC	Address Status Controller	85			56,57,66,75,78,79,95,96
CLK	Clock	89	DQa	Data Inputs/Outputs	58,59,62,63,68,69,72,73
CS1	Chip Select	98	DQb		8,9,12,13,18,19,22,23
CS2	Chip Select	97	DQPa, Pb		74,24
CS2	Chip Select	92			
WEx(x=a,b)	Byte Write Inputs	93,94	VDDQ	Output Power Supply (2.5V~3.3V)	4,11,20,27,54,61,70,77
OE	Output Enable	86	VSSQ	Output Ground	5,10,21,26,55,60,71,76
GW	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

**Function Description**

The S7B403635M and S7B401835M are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of  $\overline{OE}$ ,  $\overline{LBO}$  and  $\overline{ZZ}$ ) are sampled on rising clock edges. The start and duration of the burst access is controlled by  $\overline{ADSC}$ ,  $\overline{ADSP}$  and  $\overline{ADV}$  and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with  $\overline{ADV}$ .

When  $\overline{ZZ}$  is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When  $\overline{ZZ}$  returns to low, the SRAM normally operates after 2cycles of wake up time.  $\overline{ZZ}$  pin is pulled down internally.

Read cycles are initiated with  $\overline{ADSP}$ (or  $\overline{ADSC}$ ) using the new external address clocked into the on-chip address register when both  $\overline{GW}$  and  $\overline{BW}$  are high or when  $\overline{BW}$  is low and  $\overline{WEa}$ ,  $\overline{WEb}$ ,  $\overline{WEc}$ , and  $\overline{WEd}$  are high. When  $\overline{ADSP}$  is sampled low, the chip selects are sampled active, and the output buffer is enabled with  $\overline{OE}$ . the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with  $\overline{ADSP}$ (or  $\overline{ADSC}$ ) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.

All byte write occurs by enabling  $\overline{GW}$ (independent of  $\overline{BW}$  and  $\overline{WEx}$ ), and individual byte write is performed only when  $\overline{GW}$  is high and  $\overline{BW}$  is low. In S7B403635M, a 128Kx36 organization,  $\overline{WEa}$  controls DQa and DQPa,  $\overline{WEb}$  controls DQb and DQPb,  $\overline{WEc}$  controls DQc and DQPC and  $\overline{WEd}$  controls DQd and DQPd.

$\overline{CS1}$  is used to enable the device and conditions internal use of  $\overline{ADSP}$  and is sampled only when a new external address is loaded.

$\overline{ADV}$  is ignored at the clock edge when  $\overline{ADSP}$  is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when  $\overline{ADV}$  is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the  $\overline{LBO}$  pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

**Burst Sequence Table**

(Interleaved Burst,  $\overline{LBO}$ =High)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst,  $\overline{LBO}$ =Low)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

**Note :** 1.  $\overline{LBO}$  pin must be tied to High or Low, and Floating State must not be allowed.

**Asynchronous Truth Table**

Operation	$\overline{ZZ}$	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

**Notes**

1. X means "Don't Care".
2.  $\overline{ZZ}$  pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with  $\overline{OE}$ , otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

**Truth Tables**

**Synchronous Truth Table**

$\overline{CS}_1$	$CS_2$	$\overline{CS}_2$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{Write}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

**Notes :** 1. X means "Don't Care".

2. The rising edge of clock is symbolized by ( ↑ ).

3.  $\overline{Write} = L$  means Write operation in Write Truth Table.

$\overline{Write} = H$  means Read operation in Write Truth Table.

4. Operation finally depends on status of asynchronous input pins(ZZ and OE).

**Write Truth Table(x36)**

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	Operation
H	H	X	X	X	X	Read
H	L	H	H	H	H	Read
H	L	L	H	H	H	Write Byte A
H	L	H	L	H	H	Write Byte B
H	L	H	H	L	L	Write Byte C And D
H	L	L	L	L	L	Write All Bytes
L	X	X	X	X	X	Write All Bytes

**Notes :** 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK( ↑ ).

**Write Truth Table(x18)**

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	Operation
H	H	X	X	Read
H	L	H	H	Read
H	L	L	H	Write Byte A
H	L	H	L	Write Byte B
H	L	L	L	Write All Bytes
L	X	X	X	Write All Bytes

**Notes :** 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK( ↑ ).



**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Voltage on V <sub>DD</sub> Supply Relative to V <sub>SS</sub>	V <sub>DD</sub>	-0.3 to 4.6	V
Voltage on V <sub>DDQ</sub> Supply Relative to V <sub>SS</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V
Voltage on Input Pin Relative to V <sub>SS</sub>	V <sub>IN</sub>	-0.3 to V <sub>DD</sub> +0.3	V
Voltage on I/O Pin Relative to V <sub>SS</sub>	V <sub>IO</sub>	-0.3 to V <sub>DDQ</sub> +0.3	V
Power Dissipation	P <sub>D</sub>	1.6	W
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	Commercial	T <sub>OPR</sub>	0 to 70
	Industrial	T <sub>OPR</sub>	-40 to 85
Storage Temperature Range Under Bias	T <sub>BIAS</sub>	-10 to 85	°C

**Notes :** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Operating Conditions (0°C ≤ T<sub>A</sub> ≤ 70°C)**

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V <sub>DD1</sub>	2.3	2.5	2.7	V
	V <sub>DDQ1</sub>	2.3	2.5	2.7	V
	V <sub>DD2</sub>	3.1	3.3	3.5	V
	V <sub>DDQ2</sub>	2.3	3.3	3.5	V
Ground	V <sub>SS</sub>	0	0	0	V

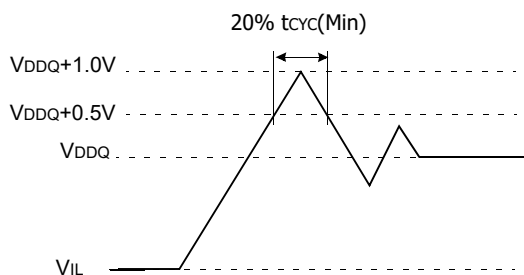
**Notes:** 1. The above parameters are also guaranteed at industrial temperature range.  
 2. It should be V<sub>DDQ</sub> ≤ V<sub>DD</sub>

**Capacitance (T<sub>A</sub>=25°C, f=1MHz)**

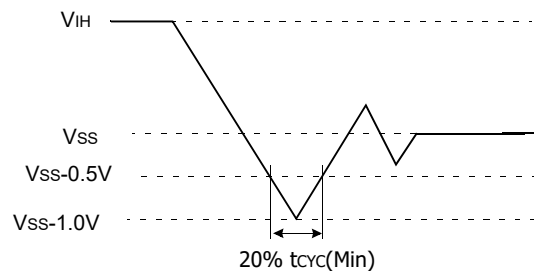
Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	5	pF
Output Capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> =0V	-	7	pF

**Note :** Sampled not 100% tested.

**Overshoot Timing**



**Undershoot Timing**



**DC Electrical Characteristics**

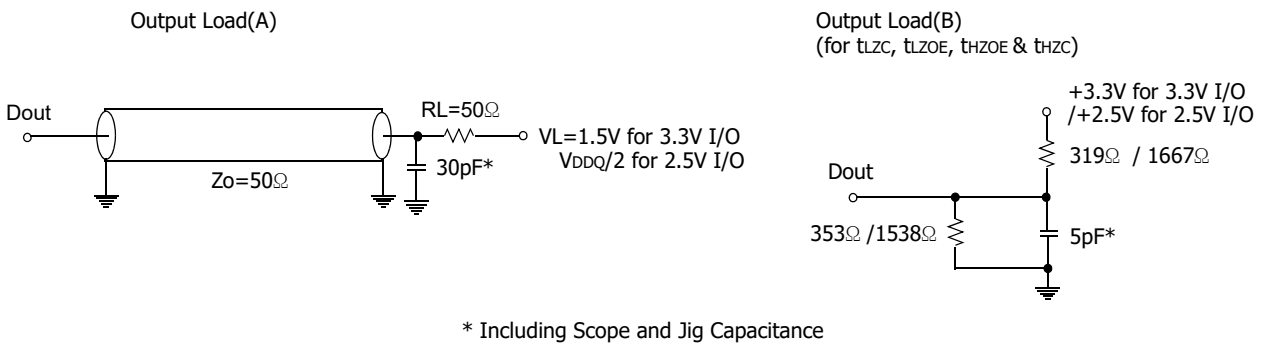
Parameter	Symbol	Test Conditions	Min	Max	Unit	Notes	
Input Leakage Current(except ZZ)	IIL	VDD=Max ; VIN=VSS to VDD	-2	+2	uA		
Output Leakage Current	IOL	Output Disabled, Vout=VSS to VDDQ	-2	+2	uA		
Operating Current	ICC	Device Selected, IOUT=0mA, ZZ ≤ VIL, Cycle Time ≥ tcyc Min	-65	-	110	mA	1,2
			-75	-	100		
Standby Current	ISB	Device deselected, IOUT=0mA, ZZ ≤ VIL, f=Max, All Inputs ≤ VIL or ≥ VIH	-	50	mA		
	ISB1	Device deselected, IOUT=0mA, ZZ ≤ 0.2V, f=0, All Inputs=fixed (VDD-0.2V or 0.2V)	-	30	mA		
	ISB2	Device deselected, IOUT=0mA, ZZ ≥ VDD-0.2V, f=Max, All Inputs ≤ VIL or ≥ VIH	-	30	mA		
Output Low Voltage(3.3V I/O)	VoL	IOL=8.0mA	-	0.4	V		
Output High Voltage(3.3V I/O)	VoH	IOH=-4.0mA	2.4	-	V		
Output Low Voltage(2.5V I/O)	VoL	IOL=1.0mA	-	0.4	V		
Output High Voltage(2.5V I/O)	VoH	IOH=-1.0mA	2.0	-	V		
Input Low Voltage(3.3V I/O)	VIL		-0.3*	0.8	V		
Input High Voltage(3.3V I/O)	VIH		2.0	VDD+0.3**	V	3	
Input Low Voltage(2.5V I/O)	VIL		-0.3*	0.7	V		
Input High Voltage(2.5V I/O)	VIH		1.7	VDD+0.3**	V	3	

**Notes :** The above parameters are also guaranteed at industrial temperature range.  
 1. Reference AC Operating Conditions and Characteristics for input and timing.  
 2. Data states are all zero.  
 3. In Case of I/O Pins, the Max. VIH=VDDQ+0.3V

**Test Conditions**

Parameter	Value
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3/2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	VDDQ/2
Output Load	See Fig. 1

The above parameters are also guaranteed at industrial temperature range.



**Fig. 1**

AC Timing Characteristics

Parameter	Symbol	-65		-75		Unit
		Min	Max	Min	Max	
Cycle Time	t <sub>CYC</sub>	7.5	-	8.5	-	ns
Clock Access Time	t <sub>CD</sub>	-	6.5	-	7.5	ns
Output Enable to Data Valid	t <sub>OE</sub>	-	3.5	-	3.5	ns
Clock High to Output Low-Z	t <sub>LZC</sub>	2.5	-	2.5	-	ns
Output Hold from Clock High	t <sub>OH</sub>	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	t <sub>LZOE</sub>	0	-	0	-	ns
Output Enable High to Output High-Z	t <sub>HZOE</sub>	-	3.5	-	3.5	ns
Clock High to Output High-Z	t <sub>HZC</sub>	-	3.8	-	4.0	ns
Clock High Pulse Width	t <sub>CH</sub>	2.5	-	2.5	-	ns
Clock Low Pulse Width	t <sub>CL</sub>	2.5	-	2.5	-	ns
Address Setup to Clock High	t <sub>AS</sub>	1.5	-	1.5	-	ns
Address Status Setup to Clock High	t <sub>SS</sub>	1.5	-	1.5	-	ns
Data Setup to Clock High	t <sub>DS</sub>	1.5	-	1.5	-	ns
Write Setup to Clock High ( $\overline{WE}$ , $\overline{BWx}$ )	t <sub>WS</sub>	1.5	-	1.5	-	ns
Address Advance Setup to Clock High	t <sub>ADVS</sub>	1.5	-	1.5	-	ns
Chip Select Setup to Clock High	t <sub>CSS</sub>	1.5	-	1.5	-	ns
Address Hold from Clock High	t <sub>AH</sub>	0.5	-	0.5	-	ns
Address Status Hold from Clock High	t <sub>SH</sub>	0.5	-	0.5	-	ns
Data Hold from Clock High	t <sub>DH</sub>	0.5	-	0.5	-	ns
Write Hold from Clock High ( $\overline{WE}$ , $\overline{BWx}$ )	t <sub>WH</sub>	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t <sub>ADVH</sub>	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t <sub>CSH</sub>	0.5	-	0.5	-	ns
ZZ High to Power Down	t <sub>PDS</sub>	2	-	2	-	cycle
ZZ Low to Power Up	t <sub>PUS</sub>	2	-	2	-	cycle

- Notes :**
1. The above parameters are also guaranteed at industrial temperature range.
  2. All address inputs must meet the specified setup and hold times for all rising clock edges whenever  $\overline{ADSC}$  and/or  $\overline{ADSP}$  is sampled low and  $\overline{CS}$  is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
  3. Both chip selects must be active whenever  $\overline{ADSC}$  or  $\overline{ADSP}$  is sampled low in order for the this device to remain enabled.
  4.  $\overline{ADSC}$  or  $\overline{ADSP}$  must not be asserted for at least 2 Clock after leaving ZZ state.

**Sleep Mode**

Sleep Mode is a low current, power-down mode in which the device is deselected and current is reduced to  $I_{SB2}$ . The duration of Sleep Mode is dictated by the length of time the ZZ is in a High state.

After entering Sleep Mode, all inputs except ZZ become disabled and all outputs go to High-Z.

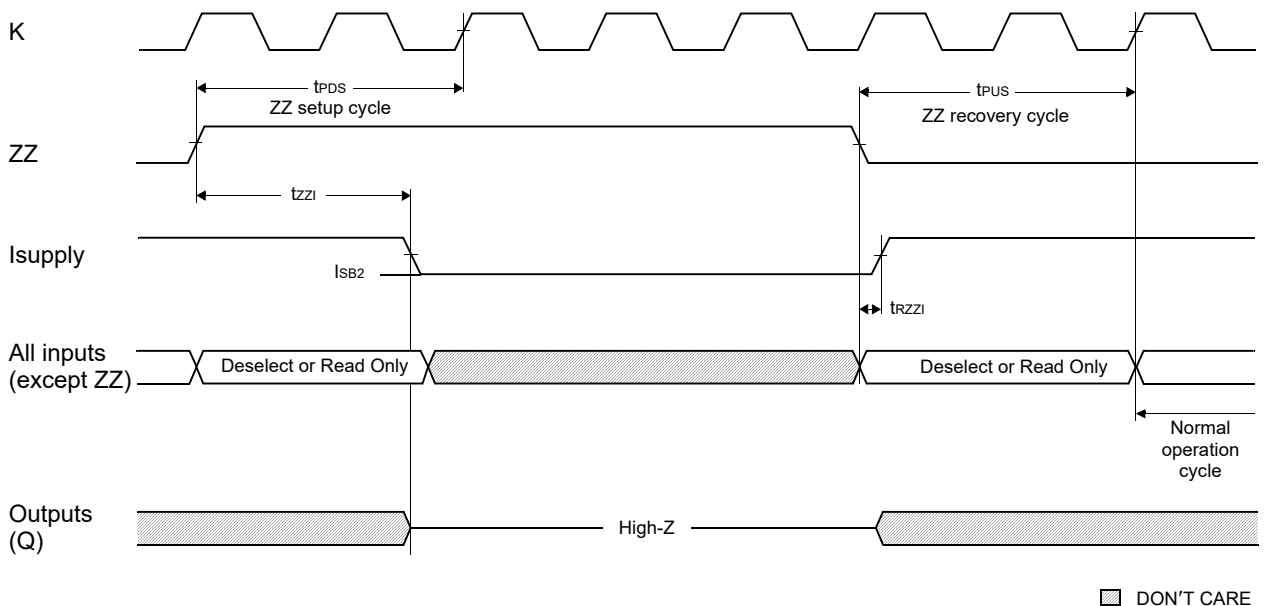
The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep Mode.

When the ZZ pin becomes a logic High,  $I_{SB2}$  is guaranteed after the time  $t_{ZZI}$  is met. Any operation pending when entering Sleep Mode is not guaranteed to successful complete. Therefore, Sleep Mode (Read or Write) must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep Mode during  $t_{PUS}$ , only a Deselect or Read cycle should be given while the SRAM is transitioning out of Sleep Mode.

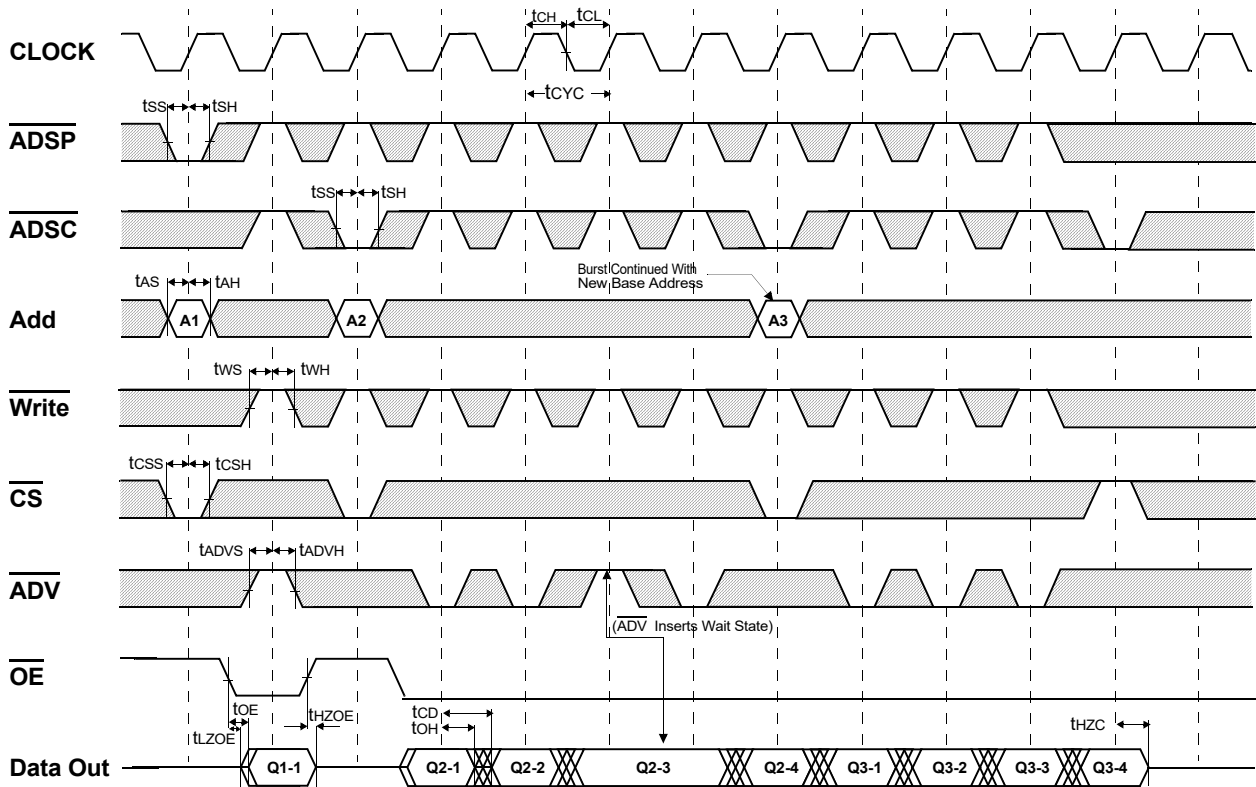
**Sleep Mode Electrical Characteristics**

Description	Condition	Symbol	Min	Max	Unit
Current during SLEEP MODE	$ZZ \geq V_{IH}$	$I_{SB2}$		30	mA
ZZ active to input ignored		$t_{PDS}$	2		cycle
ZZ inactive to input sampled		$t_{PUS}$	2		cycle
ZZ active to SLEEP current		$t_{ZZI}$		2	cycle
ZZ inactive to exit SLEEP current		$t_{RZZI}$	0		

**Sleep Mode Waveform**



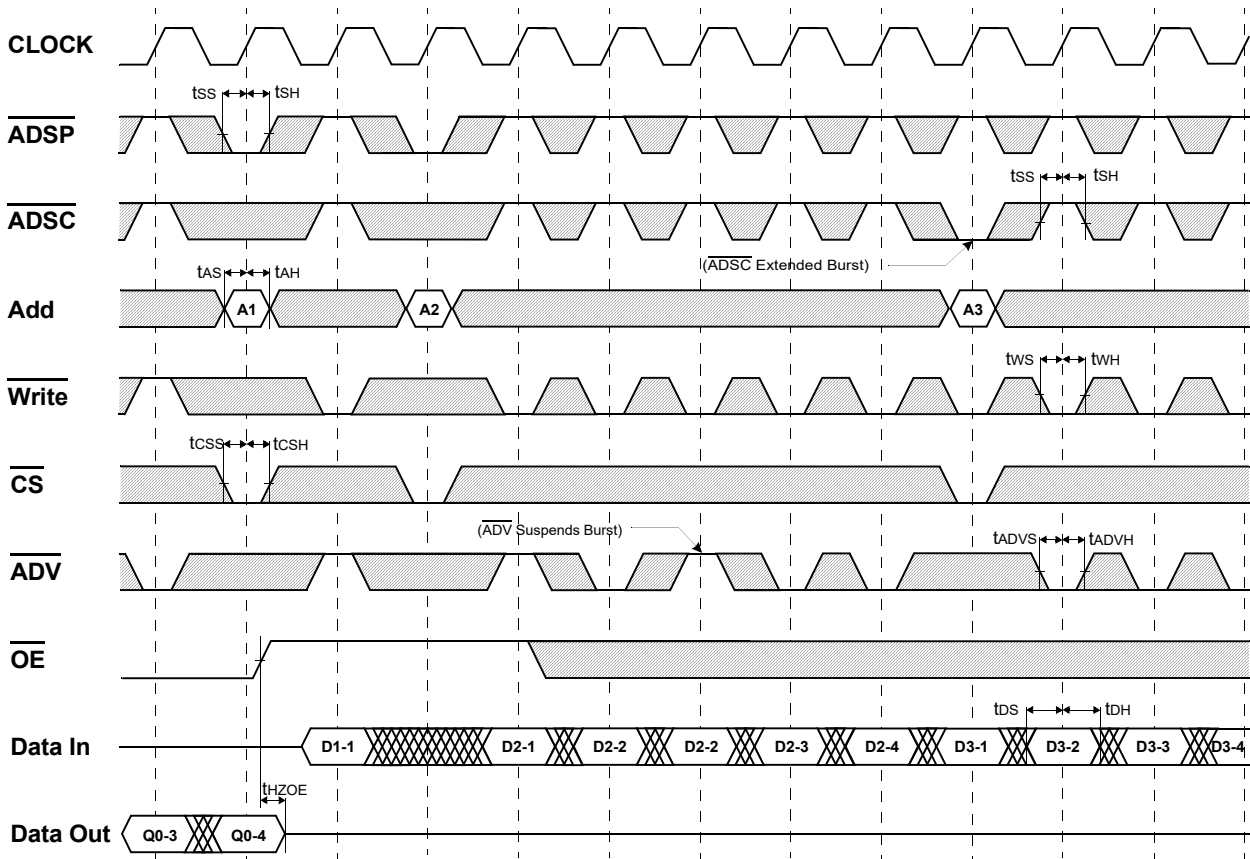
### Timing Waveform of Read Cycle



NOTES:  $\overline{\text{Write}} = L$  means  $\text{GW} = L$ , or  $\text{GW} = H$ ,  $\text{BW} = L$ ,  $\text{WEX} = L$   
 $\overline{\text{CS}} = L$  means  $\text{CS}_1 = L$ ,  $\text{CS}_2 = H$  and  $\overline{\text{CS}}_2 = L$   
 $\overline{\text{CS}} = H$  means  $\overline{\text{CS}}_1 = H$ , or  $\overline{\text{CS}}_1 = L$  and  $\overline{\text{CS}}_2 = H$ , or  $\overline{\text{CS}}_1 = L$ , and  $\text{CS}_2 = L$

□ Don't Care  
 ⊠ Undefined

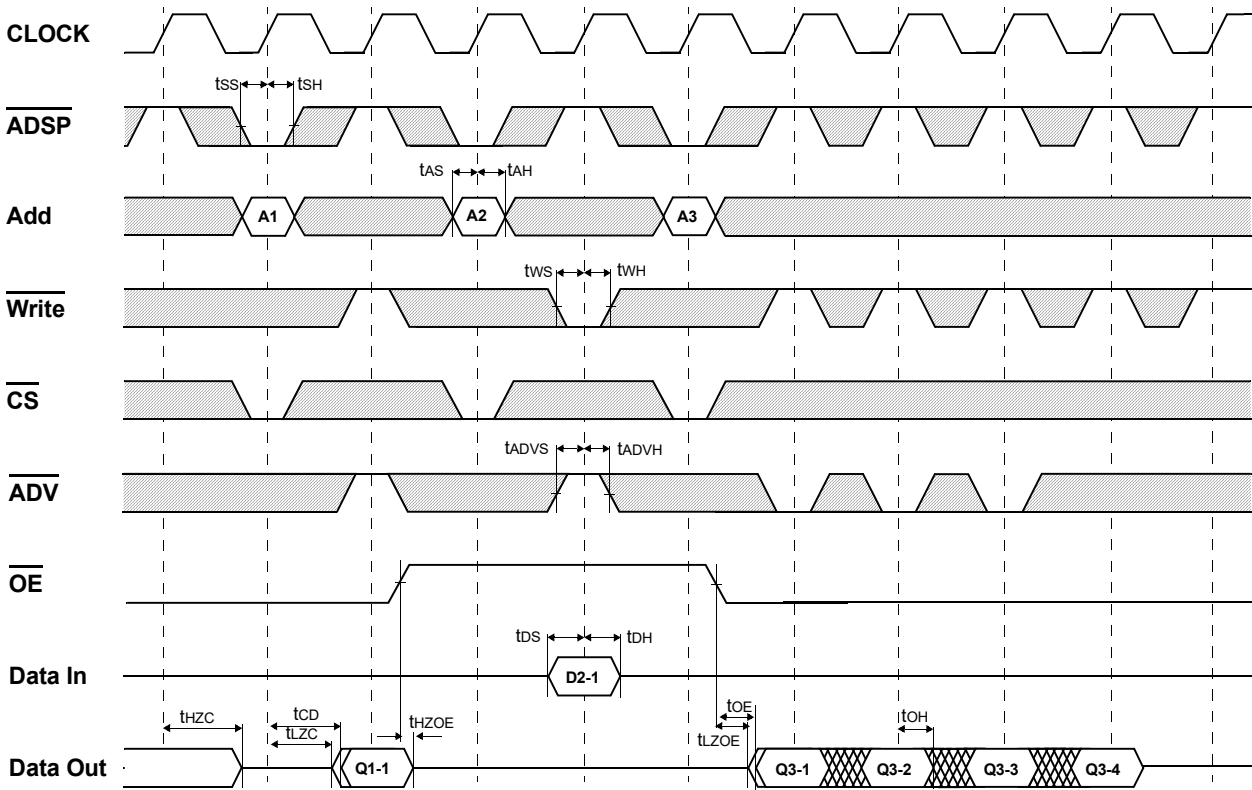
### Timing Waveform of Write Cycle



NOTES:  $\overline{\text{Write}} = \text{L}$  means  $\text{GW} = \text{L}$ , or  $\text{GW} = \text{H}$ ,  $\text{BW} = \text{L}$ ,  $\text{WEX} = \text{L}$   
 $\overline{\text{CS}} = \text{L}$  means  $\overline{\text{CS}}_1 = \text{L}$ ,  $\text{CS}_2 = \text{H}$  and  $\overline{\text{CS}}_2 = \text{L}$   
 $\overline{\text{CS}} = \text{H}$  means  $\overline{\text{CS}}_1 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$  and  $\overline{\text{CS}}_2 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$ , and  $\text{CS}_2 = \text{L}$

□ Don't Care  
 ⊗ Undefined

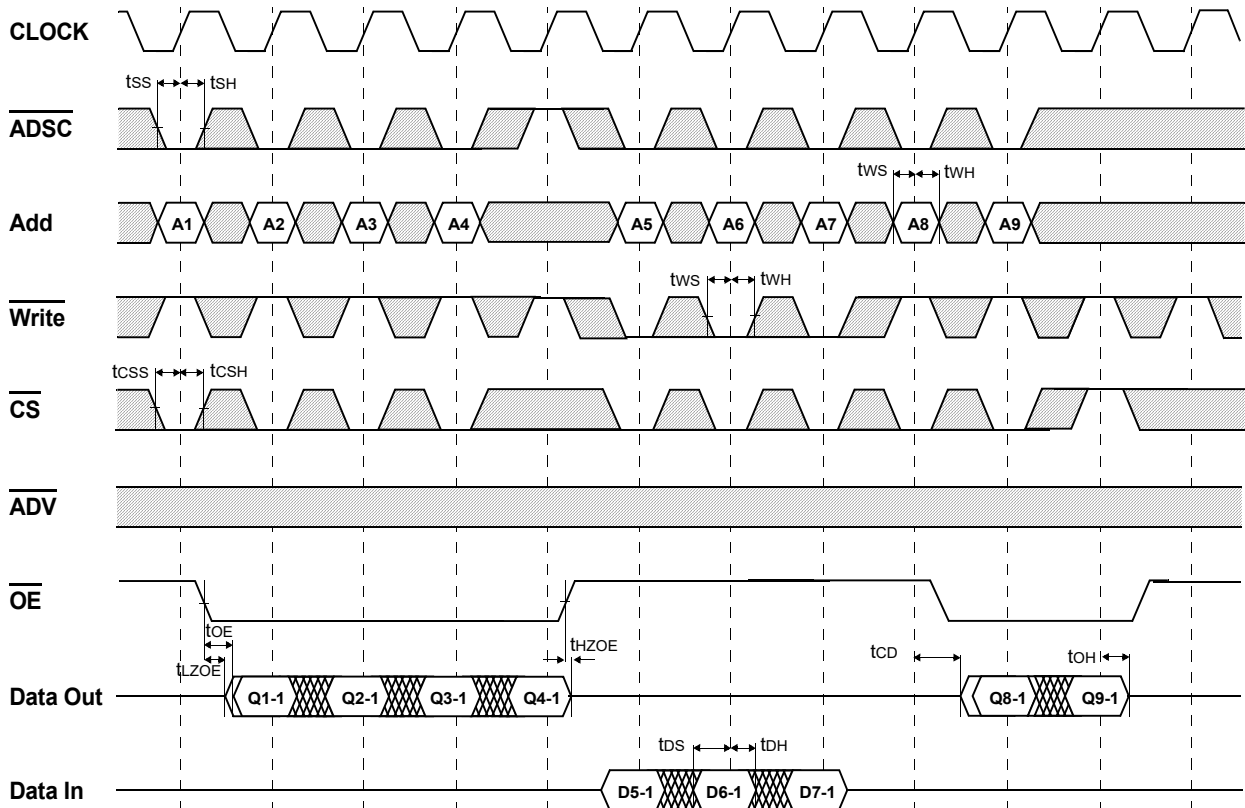
Timing Waveform of Combination Read/Write Cycle(ADSP Controlled , ADSC=High)



NOTES:  $\overline{\text{Write}} = \text{L}$  means  $\text{GW} = \text{L}$ , or  $\text{GW} = \text{H}$ ,  $\text{BW} = \text{L}$ ,  $\text{WEX} = \text{L}$   
 $\overline{\text{CS}} = \text{L}$  means  $\overline{\text{CS}}_1 = \text{L}$ ,  $\text{CS}_2 = \text{H}$  and  $\overline{\text{CS}}_2 = \text{L}$   
 $\overline{\text{CS}} = \text{H}$  means  $\overline{\text{CS}}_1 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$  and  $\overline{\text{CS}}_2 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$ , and  $\text{CS}_2 = \text{L}$

□ Don't Care  
 ▣ Undefined

Timing Waveform of Single Read/Write Cycle ( $\overline{\text{ADSC}}$  Controlled,  $\overline{\text{ADSP}}=\text{High}$ )

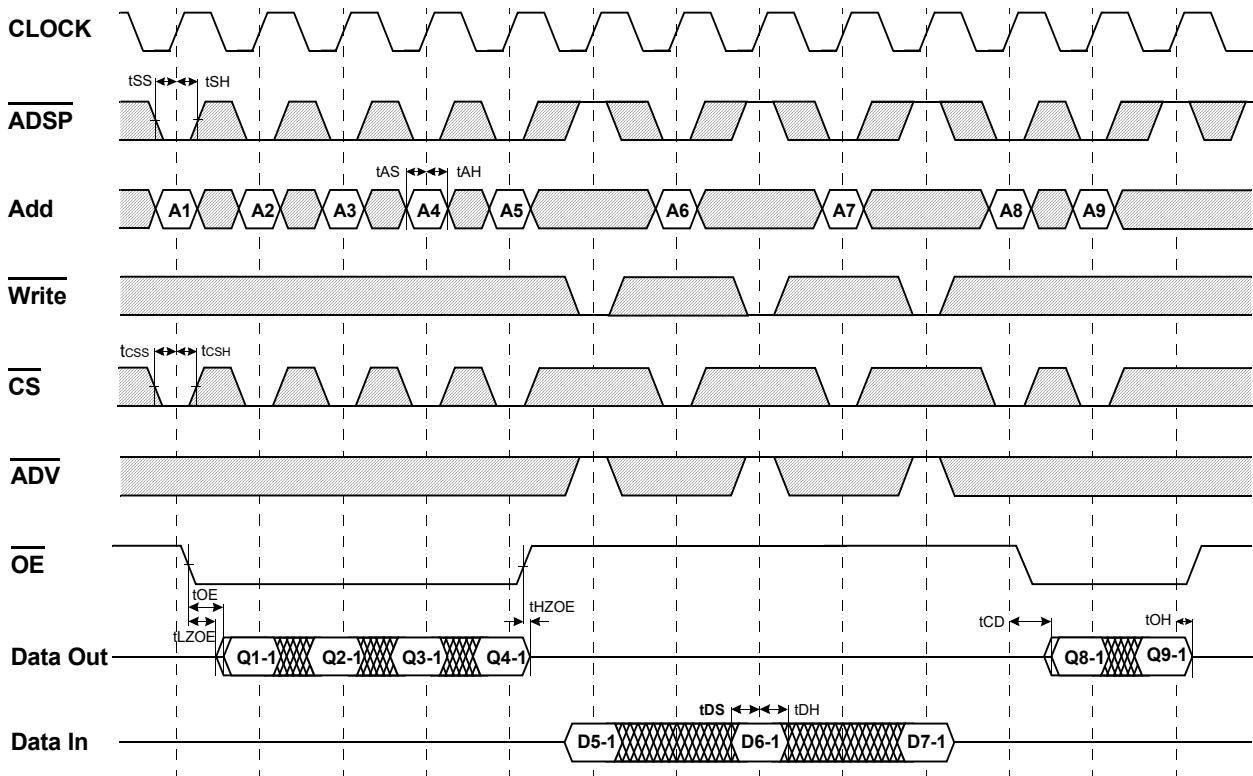


NOTES:  $\overline{\text{Write}} = \text{L}$  means  $\text{GW} = \text{L}$ , or  $\text{GW} = \text{H}$ ,  $\text{BW} = \text{L}$ ,  $\text{WEX} = \text{L}$   
 $\overline{\text{CS}} = \text{L}$  means  $\overline{\text{CS}}_1 = \text{L}$ ,  $\text{CS}_2 = \text{H}$  and  $\overline{\text{CS}}_2 = \text{L}$   
 $\overline{\text{CS}} = \text{H}$  means  $\overline{\text{CS}}_1 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$  and  $\overline{\text{CS}}_2 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$ , and  $\text{CS}_2 = \text{L}$

□ Don't Care  
 X Undefined



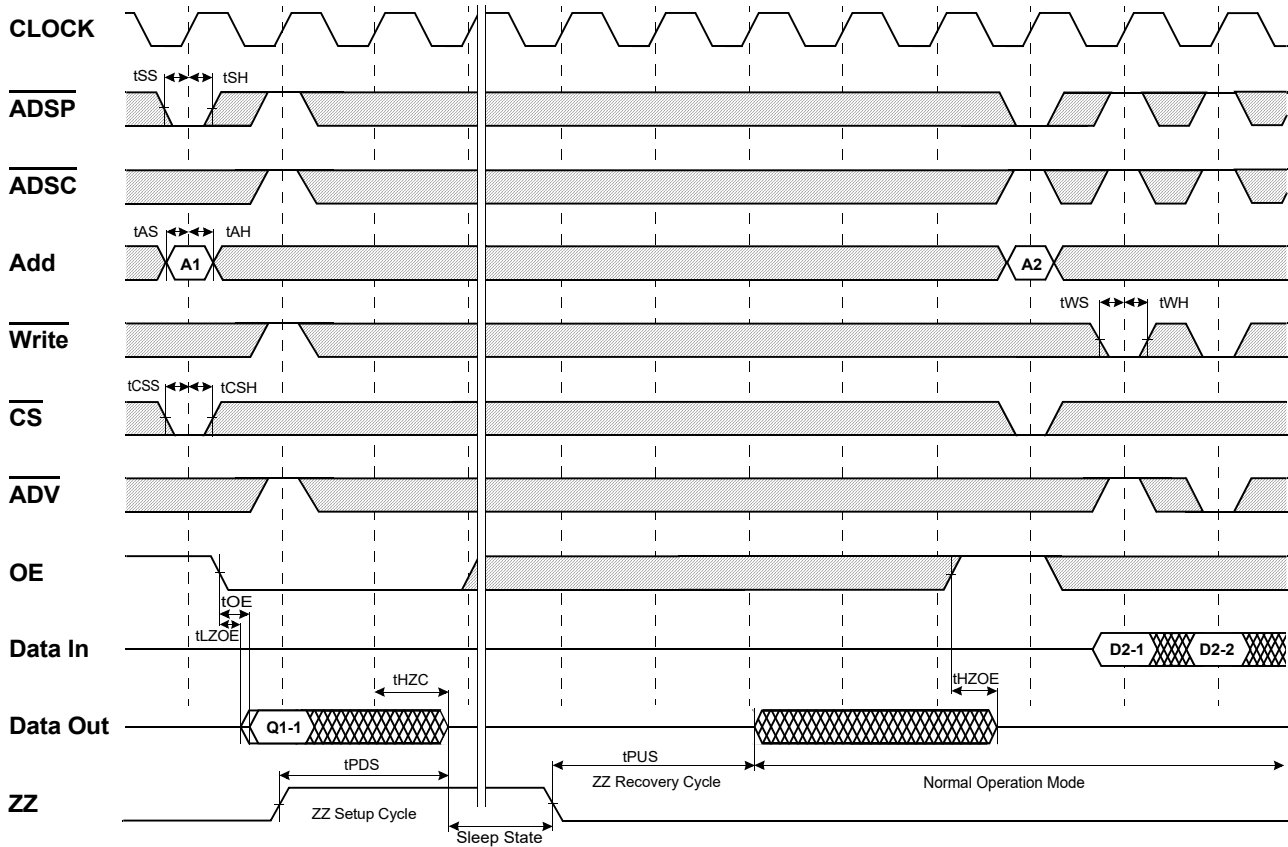
Timing Waveform of Single Read/Write Cycle ( $\overline{\text{ADSP}}$  Controlled,  $\overline{\text{ADSC}}=\text{High}$ )



NOTES:  $\overline{\text{Write}} = \text{L}$  means  $\text{GW} = \text{L}$ , or  $\text{GW} = \text{H}$ ,  $\text{BW} = \text{L}$ ,  $\text{WEx} = \text{L}$   
 $\overline{\text{CS}} = \text{L}$  means  $\overline{\text{CS}}_1 = \text{L}$ ,  $\text{CS}_2 = \text{H}$  and  $\overline{\text{CS}}_2 = \text{L}$   
 $\overline{\text{CS}} = \text{H}$  means  $\overline{\text{CS}}_1 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$  and  $\overline{\text{CS}}_2 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$ , and  $\text{CS}_2 = \text{L}$

□ Don't Care  
 ▨ Undefined

Timing Waveform of Power Down Cycle



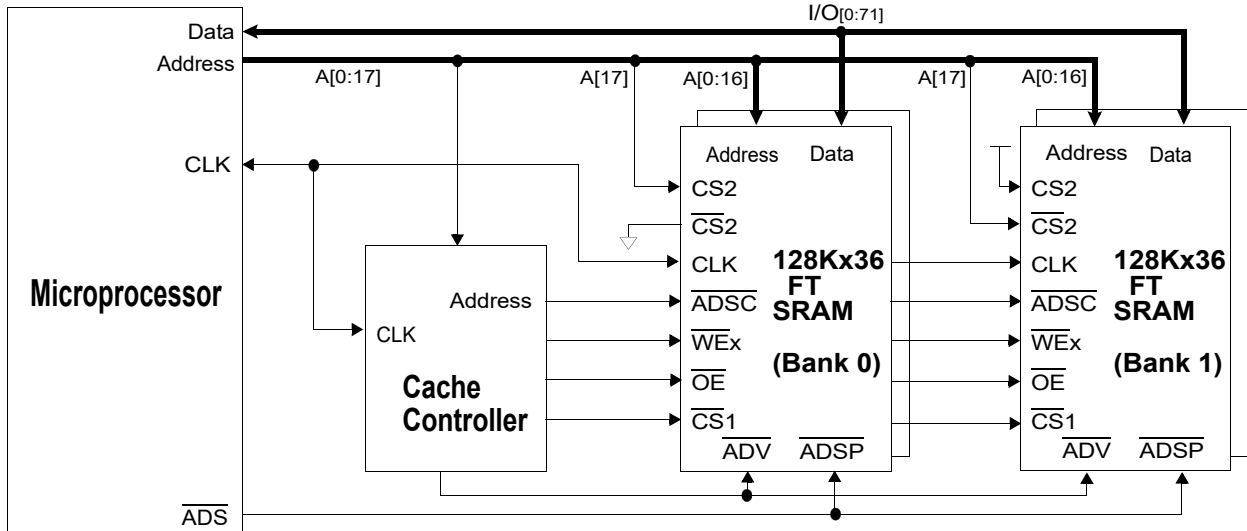
NOTES:  $\overline{\text{Write}} = \text{L}$  means  $\overline{\text{GW}} = \text{L}$ , or  $\overline{\text{GW}} = \text{H}$ ,  $\overline{\text{BW}} = \text{L}$ ,  $\overline{\text{WEx}} = \text{L}$   
 $\overline{\text{CS}} = \text{L}$  means  $\overline{\text{CS1}} = \text{L}$ ,  $\overline{\text{CS2}} = \text{H}$  and  $\overline{\text{CS2}} = \text{L}$   
 $\overline{\text{CS}} = \text{H}$  means  $\overline{\text{CS1}} = \text{H}$ , or  $\overline{\text{CS1}} = \text{L}$  and  $\overline{\text{CS2}} = \text{H}$ , or  $\overline{\text{CS1}} = \text{L}$ , and  $\overline{\text{CS2}} = \text{L}$

□ Don't Care  
 ▨ Undefined

Application Information

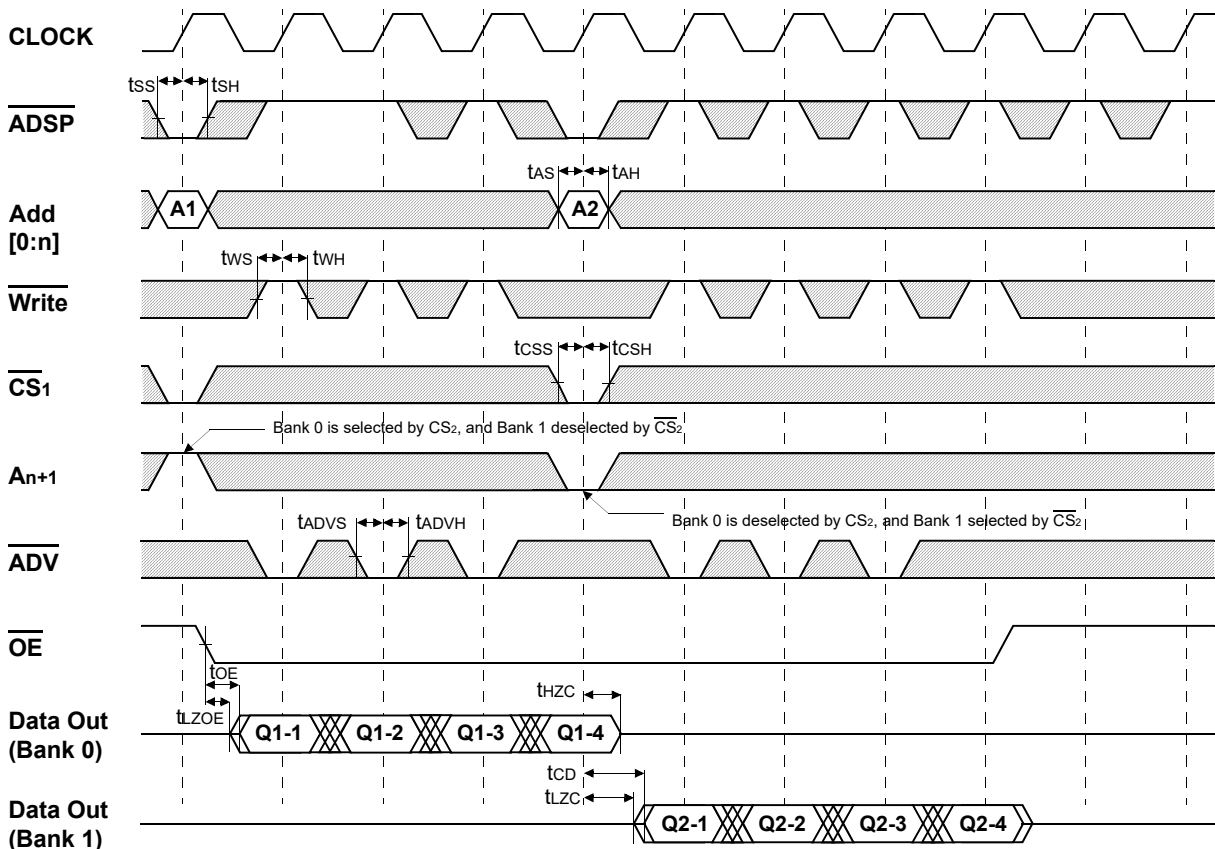
Depth Expansion

The Netsol 128Kx36 Flow-Through SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 128K depth to 256K depth without extra logic.



Interleave Read Timing (Refer to non-interleave write timing for interleave write timing)

(ADSP Controlled, ADSC=HIGH)



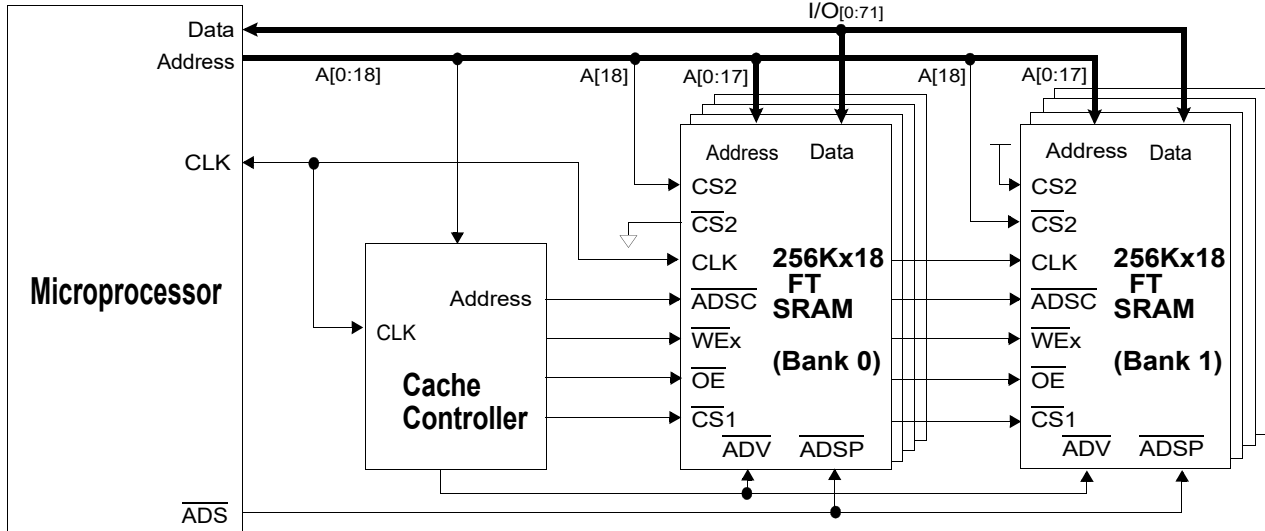
Notes : n = 14 32K depth, 15 64K depth  
16 128K depth, 17 256K depth

□ Don't Care    ⊗ Undefined

Application Information

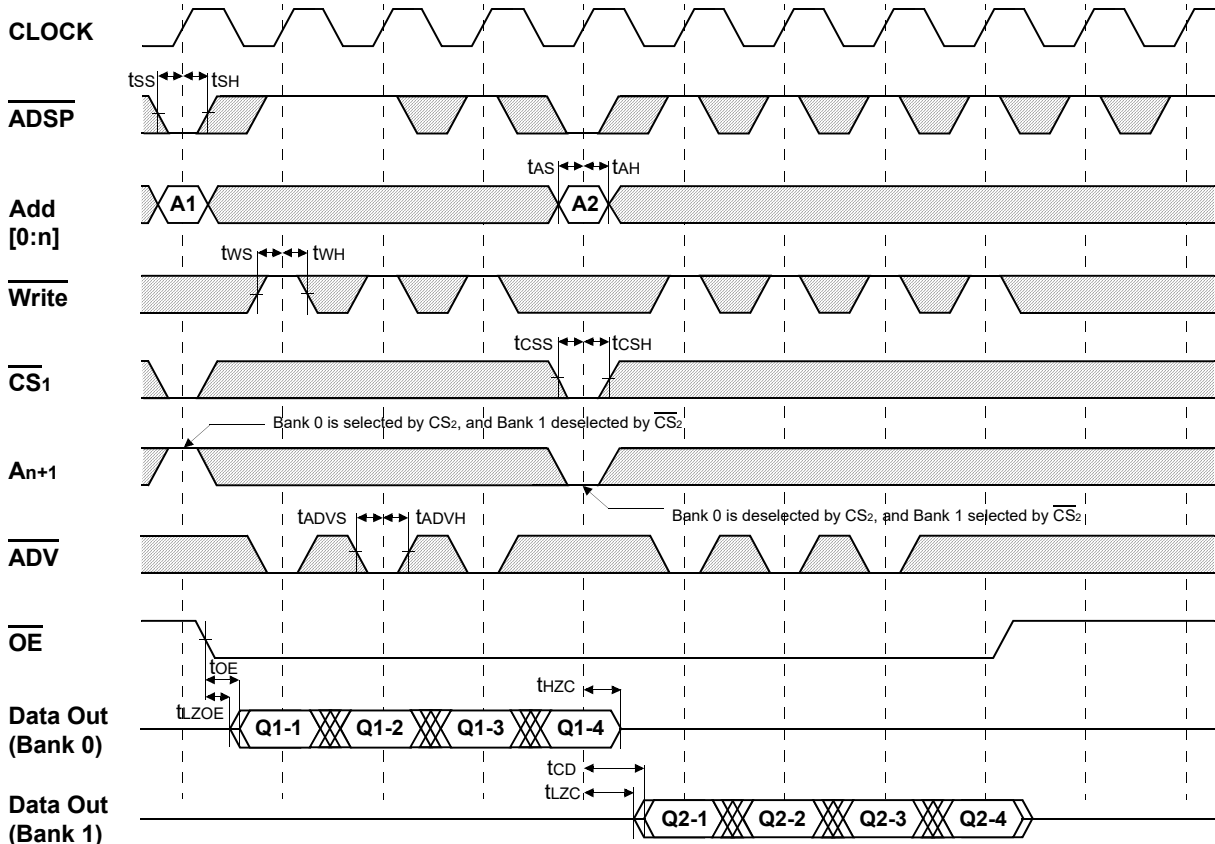
Depth Expansion

The Netsol 256Kx18 Flow-Through SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 256K depth to 512K depth without extra logic.



Interleave Read Timing (Refer to non-interleave write timing for interleave write timing)

(ADSP Controlled, ADSC=HIGH)



Notes : n = 14 32K depth, 15 64K depth  
16 128K depth, 17 256K depth

□ Don't Care    ⊗ Undefined

Package Dimensions

